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LOW POWER RF SINGLE BALANCED MIXER WITH HIGH CONVERSION GAIN FOR ISM BAND APPLICATIONS

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Abstract

This paper involves the design and simulation of a single balanced down conversion mixer from a Gilbert cell mixer using a source degeneration inductor and folded structure in 65nm CMOS Technology. The proposed single balanced mixer operating at a radio frequency (RF) 2.4GHz attain a high conversion gain of 25.39dB, RF to IF isolation value of -22.636dB, third order intercept point (IIP3) of 32dBm, Noise Figure (NF) of 9.236dB at IF port and 1-dB compression point of -18.013dBm. The power consumed by the mixer circuit is 5.5mW with the supply voltage of 0.8V.

Keywords:

Mixer; Single Balanced; Noise Figure; Isolation; Linearity

1. INTRODUCTION

Low power radio frequency (RF) applications like ZigBee or Bluetooth are taking the market areas of low cost short range communications. Practical applications of the low frequency wireless standards includes wireless sensor networks, industrial, scientific, medical and personal uses working on just batteries. All the practical applications require low-cost chip solutions [1].

In the RF front-end receiver as shown in Fig.1 the down-conversion mixer is one of the important component used to convert an input radio frequency (RF) signal to an output intermediate frequency (IF) signal.

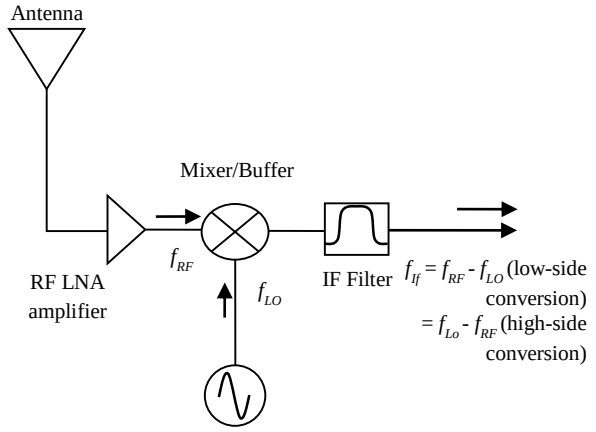

Fig.1. RF Front End Receiver

Basically mixers can be implemented using any of the nonlinear devices like diodes, Field Effect Transistors (FET) and bipolar transistors (BJT). Mixer can be classified into two types. They are passive and active mixers. In comparison to the active topologies, the passive mixer does not provide high conversion gain because they are lossy in nature. But passive mixer tends to achieve better linearity. The passive mixer aims to minimize the conversion loss, because low conversion loss guarantees low-noise operation. In microwave FET mixers, high conversion gain is relatively easy to obtain, but it does not automatically insure that other aspects of performance will be good. In most of the cases, high mixer gain is often not necessary in receivers because it tends to increase the distortion of the entire receiver. Hence an active mixer is designed not to achieve the maximum possible gain, but to achieve a low noise figure and modest gain [2].

In order to retrieve the desired message signal, it is necessary to perform a frequency conversion by a mixer which allows a time multiplication of two signals, RF signal (coming from the receiver antenna after has been filtered and amplified) and local oscillator (LO) signal, the result is a transposition of a high or a low intermediate frequency (IF) with a minimum of a magnitude loss and a minimal noise figure.

In order to convert a high radio frequency signal to low frequency intermediate signal, the RF signal is subtracted from local oscillator (LO) signal or vice versa as shown in Eq.(1) and Eq.(2) below. RF Mixers generates frequencies not present at their input and used together with appropriate filtering they remove unwanted frequencies.

$$f_{IF} = f_{RF} - f_{LO} \text{ (for low side conversion)} \quad (1)$$

$$f_{IF} = f_{LO} - f_{RF} \text{ (for high side conversion)} \quad (2)$$

Many forms of mixer are not balanced and as a result they allow considerable levels of the local oscillator and RF signals at output. These are normally not necessary and normally they would have to be removed by filtering process which is difficult and expensive. One of the solutions to balance the mixer is to remove the input signals either RF or LO. One type of balanced mixer that is commonly used is single balanced mixer that suppress either the LO or RF signal at the output but not both.

2. RELATED WORKS

Various types of RF mixer topologies realized using CMOS and Bi-CMOS Technologies are presented in [3] with their parameters compared between various topologies. The single-balanced mixer in shown in Fig.2 is the simplest approach that can be implemented in most semiconductor processes.

The work presented in [4] designs a Single Balanced Mixer (SBM) with the 65nm CMOS technologies for a 1.9GHz RF frequency from a Gilbert cell mixer for wireless applications and compares with other mixers with various CMOS technologies. However with the smallest CMOS Technology it achieves a low conversion gain.

A wideband down-conversion mixer designed in TSMC 0.18µm CMOS process is presented in [5] based on g_m-boosting and the current-bleeding techniques. These techniques primarily improve linearity of the mixer. This mixer operates over the entire

1.4-3.6GHz LTE-advanced bands achieve a high linearity with moderate conversion gain.

The original multiplier principle of the Gilbert cell mixer [6] targeted at sinusoidal signal for both RF and LO inputs. The LO signal is assumed to be the small signal compared to RF signal for most of the cases while using Gilbert mixer. In the mixers designed based on Gilbert Cell mixers that are used nowadays, the LO signal is chosen large enough so that the LO stage transistors alternately commutate all of the tail current from one side to the other at the LO frequency. It is more or less equivalent of using a square wave as the LO signal to modulate the RF signal. Although the square wave introduces a lot of odd undesirable harmonics that are to be filtered out with the IF filters.

A Gilbert-cell mixer in 0.13µm CMOS technology is presented in [7] operating in a wideband of 9GHz to 50GHz. The mixer was implemented in a differential configuration here so on-chip transformer baluns were used to convert the single ended RF and LO signals into differential signals. The buffers at the output were used to drive 50Ω of load. The trans-conductance (g_m) of the transistors in RF stage was increased by using current injection technique to improve the overall noise performance. But using transformers may increase the size and power consumption of the circuit.

A CMOS integrated image reject front-end presented in [8] is capable of operating in 950MHz. It consists of an image reject LNA and a single-balanced active mixers with resistive loads and source degeneration inductor that enables a high IF frequency for down conversion. The 0dBm of LO power drives into both sides of the mixer that can easily switch the MOS transistors from their saturation region to their cutoff region and vice versa without overdriving the mixer. Because the mixer core transistors are biased near threshold voltage allowing the mixer to operate with very low voltage supply leading to slightly increasing distortion. The mixer suffers from distortion and the high value inductor present may increase the size of receiver.

There has been a lot of growth in the field of mixer circuits with the introduction of Metal Oxide Semiconductor Field Effect Transistors (MOSFET). The most popular configuration of FET based mixer circuit is the Gilbert-cell mixer [9]. This mixer can be designed and implemented by using either bipolar transistors or field-effect transistors. Depending on the current source employed and the two stacked transistors, the Gilbert cell mixer circuit is difficult to implement for low supply and low- power applications. The noise figure of conventional Gilbert cell mixer is normally high because of the increased number of active devices and resistors. If this mixer is to be implemented using discrete components then it requires a matching network designed using on-chip capacitors or inductor for obtaining high input impedance.

The RF front End circuit operating in 2.4GHz composed of low noise amplifier (LNA) and down conversion mixer is described in [10]. The LNA's designed in [10] are cascade single-ended and differential. The mixer is an inductively coupled type. The mixer uses a gate and source degeneration inductor that achieves a better impedance match and reduces the flicker noise.

A RF front-end transceiver chipset for dual band applications operating in 1.86GHz and 2.14GHz implemented in a 0.25µm single-poly CMOS technology is presented in [11]. The receiver IC consists of a low noise amplifier and a down conversion mixer and the transmitter IC integrates an up-mixer. The down conversion mixer in [11] is designed without the LO processing circuit containing three-stage configuration. The first stage is single to differential amplifying balun, next is the double-balanced Gilbert cell mixer and last stage is an output driver. The LO buffer is used to switched on or off the circuits depending on the status of the transceiver modes.

The single balanced mixer designed in 0.18µm in [12] uses a separate biasing circuit along with current mirror topology for the RF stage that operates in 1.9GHz has low conversion gain even though it obtained a low power consumption and noise figure.

A RF mixer operating in 2.4GHz for ISM band applications in [13] is designed using common mode feedback circuit and modified class-AB trans-conductor stage. The class-AB trans-conductor stage provides a less degradation of linearity parameters like third order intercept point and 1dB compression point compared to the differential pair stages.

An integrated CMOS ultra low power single balanced down conversion active mixer presented in [14] is designed from a Gilbert-cell based on a resistor-loaded topology that is capable operating in 2.4GHz with all of the MOS transistors of mixer core are biased in sub-threshold region. This mixer achieves a high gain and better linearity but the noise figure of the mixer is high.

3. DESIGN

The conventional architecture for single balanced mixer [4] is shown in Fig.2 consists of two identical NMOS transistors M2 and M3 with differential input on local oscillator stage. The output current is controlled by the state of the VCO signal generated by the local oscillator. It also contains a single NMOS transistor for RF Stage. But the RF signal is not a differential one. The RF input signal changes the drain-source current (I_{DS1}) of transistor M1. The switching operations of transistors M2 and M3 increments this change in I_{DS1} of M1 with the help of input LO signal.

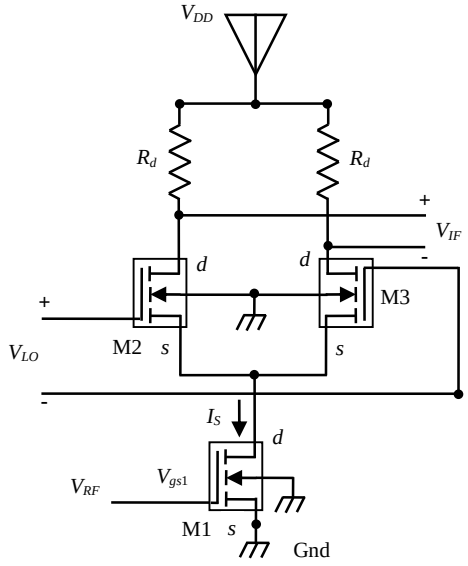

Fig.2. Conventional Single Balanced Mixer

The proposed work involves the design of down conversion mixer as shown in Fig.3 by including [8] a source degeneration inductor L_1 (2nH) to the transistor M1 and M2 at RF input stage. The inductor value must be low because high value inductors may

increase the size. The RF stage consists of a folded structure with two transistors (M1 and M2) but usually a single balanced mixer has one transistor in RF stage. The single ended RF input (V_{RF}) of 2.4GHz is provided to the transistor M1 only of RF stage for improving linearity and gain, while M2 is provided with only DC voltage. The local oscillator stage consists of two NMOS transistors M3 and M4 connected in a folded structure similar to conventional mixer. The LO input (V_{LO}) is only differential and RF input is single ended. The output intermediate frequency signal V_{IF} is obtained by the voltage between the drains of CMOS M3 and M4. The CMOS process of the proposed mixer is 65nm Technology.

The use of folded technique in mixer [10] is only to increase the bias current through the trans-conductance stage without increasing the current through the switching transistors. It needs smaller LO drive voltage to drive the switching transistors and thereby improves the switching efficiency. To provide better impedance matching at the input and to reduce the noise figure an inductor $L1$ is included in the RF input stage.

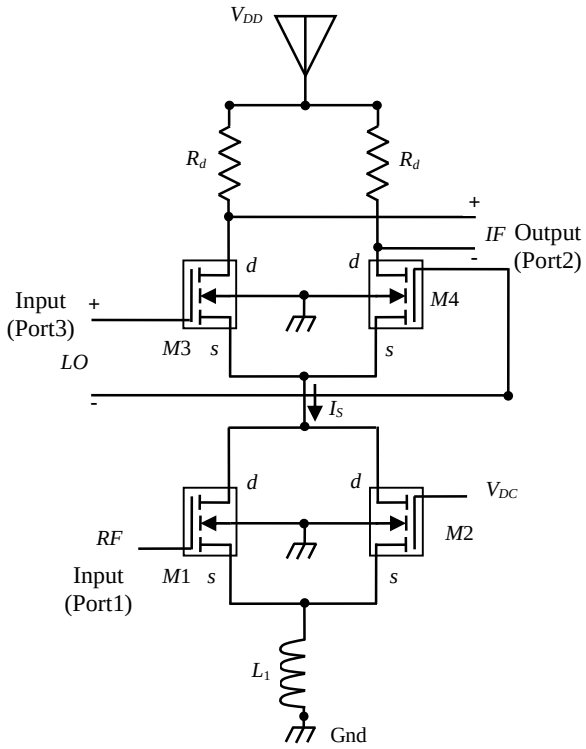

Fig.3. Proposed Single balanced Mixer

The drain resistors R_d used in the proposed mixer have low resistance values of 100Ω due to the fact that when the combination of the parasitic bond and package inductance and the parasitic pad and gate capacitance creates series resonance [11]. But these resistors are primarily used for input matching. The mixer [11] with the folded structure has high number of inductors than the proposed one.

The RF frequency is 2.4GHz and Local Oscillator (LO) frequency is 2.3GHz are the chosen frequencies for the proposed mixer to obtain an intermediate frequency of 100MHz Since the RF frequency is the higher frequency the Low side local oscillator conversion is done as depicted in the Fig.3. The intermediate frequency is 100MHz obtained by determining the difference between the RF and LO frequencies. The width of the transistor is evaluated by [10] using this Eq.(3) shown below,

$$W = \frac{g_m^2 L}{2K_n I_{DS}} \tag{3}$$

where, L is the channel length of the transistor, I_{DS} is the drain to source current and g_m is the trans-conductance. K_n is the process dependent term. The spectrum for a mixer with low side LO conversion is shown in Fig.4 having high RF frequency than LO frequency.

The gate length of all NMOS transistors used is 0.065µm, while the gate width of transistors M2 and M4 is 40µm, M1 and M3 is 100µm.

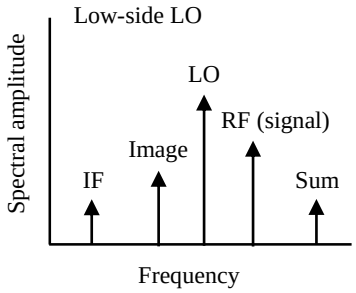

Fig.4. Spectrum for Low Side conversion of mixer

V_{gs1} is the bias voltage for M1 and it is the DC component for RF stage, V_{DC} is the bias voltage for M2, V_{gs2} is the bias voltage for differential pair of transistors M3 and M4 in LO stage.

The proposed single balanced mixer architecture with the two transistors of the differential pair at LO stage is in switching mode [12]. Therefore the current output is controlled by the local oscillator signal given by Eq.(4):

$$I_{out} = I_s(t)sign[V_{LO}(t)] \tag{4}$$

The source current $I_s(t)$ from LO stage to RF stage is given by [4] in Eq.(5),

$$I_s(t) = g_m V_{gs1} + g_m V_{RF}\cos(\omega_{RF}t) \tag{5}$$

The V_{IF} and I_{IF} of the intermediate frequency spectrum can be obtained [4] as written in Eq.(6) and Eq.(8).

$$I_{IF}(t) = \left\{g_m V_{gs1} + g_m V_{RF}\cos(\omega_{RF})\right\} \times \frac{4}{\pi} \times \left\{\cos(\omega_{LO}t) - \frac{1}{3}\cos(3\omega_{LO}t) + \frac{1}{5}\cos(5\omega_{LO}t) + \ldots\right\} \tag{6}$$

$$V_{IF}(t) = R_d \times I_{IF}(t) \tag{7}$$

$$V_{IF}(t) = \left\{\frac{4g_m V_{gs1}}{\pi} R_d \cos(\omega_{LO}t) + \frac{2}{\pi} R_d g_m V_{RF} \left[\cos((\omega_{RF} - \omega_{LO})t) - \cos((\omega_{RF} + \omega_{LO})t) + \ldots\right]\right\} \tag{8}$$

4. SIMULATION RESULTS

The mixer is designed and simulated using Advanced Design System tool to determine parameters that evaluates the performance of mixers are conversion gain or loss, linearity parameters, noise figure, port to port isolations and power consumption. The harmonic balance simulation (with order 6) in ADS tool is used to obtain the output intermediate frequency (IF)

spectrum of the proposed mixer as shown in Fig.5 below. The values of V_{gs1}, V_{DC} and V_{gs2} used in simulation are 0.5V, 0.4V and 0.5V. The RF power is -11.5dBm and the LO power is 10dBm.

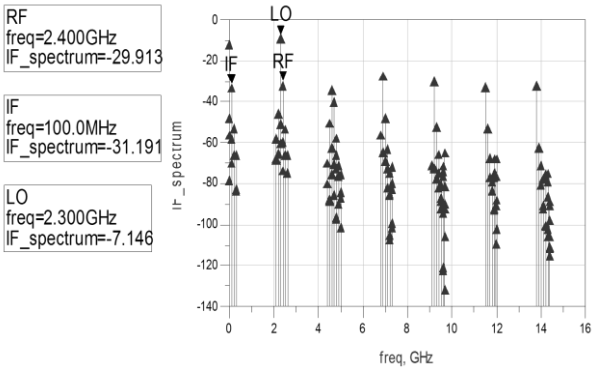

Fig.5. IF Spectrum of proposed mixer

Conversion Gain (CG) or Loss is the ratio of the desired IF output (voltage or power) to the RF input signal value (voltage or power) as represented in Eq.(9). The RF input and IF output responses are represented in the Fig.6 and Fig.7.

$$\mathrm{CG(dB)} = \frac{\mathrm{IF_{Power}(dB)}}{\mathrm{RF_{Power}(dB)}} \tag{9}$$

The conversion gain of the proposed mixer [4] is represented in an Eq.(10) below,

$$\mathrm{CG(dB)} = \frac{V_{IF_{at(\omega_{RF}-\omega_{LO})}}}{V_{RF_{at(\omega_{RF})}}} = \frac{2}{\pi} R_d g_m \tag{10}$$

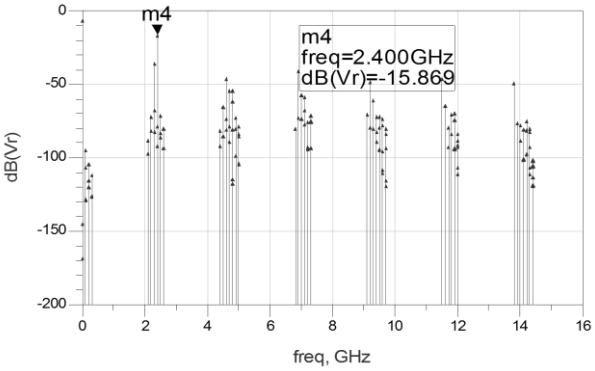

Fig.6. Input RF Response

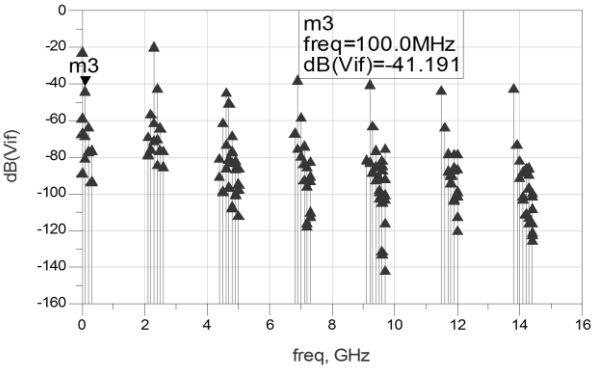

Fig.7. Output IF Response

The conversion gain of the proposed mixer circuit can be calculated by using the Eq.(9). The input RF response and Output IF response is depicted in figures shown above in Fig.6 and Fig.7.

CG = (-15.8dB) - (-41.191dB) = 25.39dB

The trans-conductance (g_m) value is 16mA/V obtained through simulation and the conversion gain can be theoretically calculated using Eq.(10).

Isolation is the amount of local oscillator power that leaks into either the IF or the RF ports. There are multiple types of isolation between the ports like LO-to-RF, LO-to-IF and RF-to-IF isolation having the minimum values of -30.958dB, -19.570dB and -22.636dB. The isolation between the LO-to-RF ports, LO-to-IF ports and RF-to-IF ports are depicted in the Fig.8, Fig.9 and Fig.10.

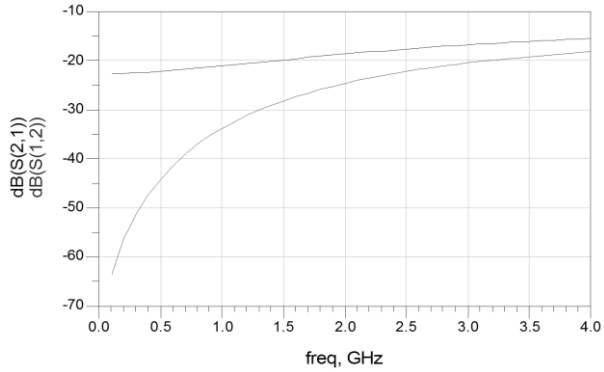

Fig.8. RF to IF Port Isolation

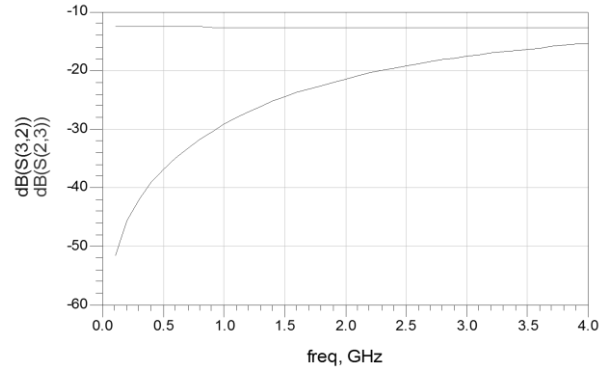

Fig.9. LO to IF Port Isolation

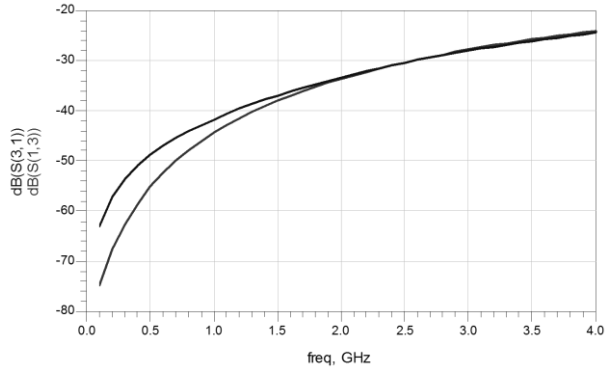

Fig.10. LO-to-RF Isolation

Noise Figure (NF) is a measure of the noise added by the Mixer itself, noise as it gets converted to the IF output. The noise figure of a mixer is measured in terms of degradation of signal to noise ratio between the input and the output ports.

$$NF = \frac{N_{IF}}{N_{RF}.CG} \tag{11}$$

The noise figure at the IF port and RF port is 9.236dB and 8.828dB as shown in Fig.11. Hence the overall noise figure can be calculated using the Eq.(11).

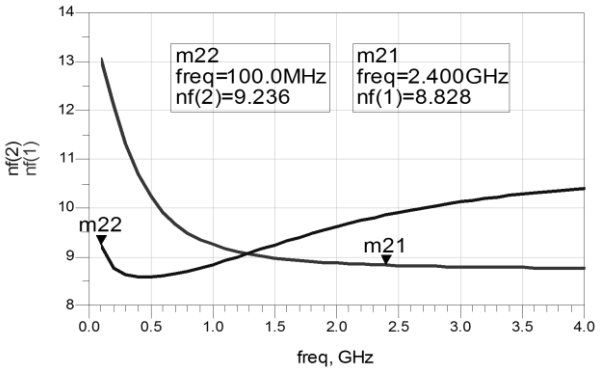

Fig.11. Noise Figure

Double Sideband (DSB) Noise Figure includes noise and signal contributions at both the RF and the image frequencies. No image signal is included in calculating Single Sideband (SSB) Noise Figure although image noise is included. The DSB and SSB noise figure values obtained by simulating the proposed mixer are 29dB and 30dB.

Third Order Intercept Point is a figure of merit for mixer that gives an indication of the mixer's signal handling capability. In particular it provides an indication of the levels of third order products a mixer that is likely to be produced under multi-tone excitation. It is measured by applying two closely spaced input tones at frequencies F_1 and F_2.

In a down conversion mixer, the third order products are $(2F_1\text{-}F_2)$ - F_{LO} and $(2F_2\text{-}F_1)\text{-}F_{LO}$ as they fall closer to the IF band. Fig.12 depicts the IF output spectrum of a down convert mixer under two-tone excitation.

The third order intercept point (IIP3) is an imaginary point, at which the third order product becomes as large as the direct down converted product. The level of the third order products rises at three times the rate of increase of the input signal level and fundamental output level. The mixer's output referred third order intercept point (TOI_{out}) can be measured using the Eq.(12), in dB.

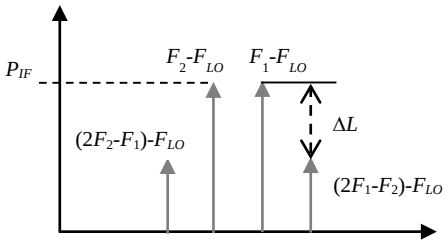

Fig.12. IF Spectrum for mixer third order Intercept point measurement

$$TOI_{out} = P_{IF} + \frac{\Delta L}{2} \tag{12}$$

The simulation result shows that the linearity parameters of proposed mixer such as third order intercept point (IIP3) and -1dB compression point values are 32dBm and -18.013dBm. The linearity of a mixer refers to its signal level handling ability. Thus a mixer with high linearity will have a high IIP3.

Table.1. Performance Comparison between the Parameters of the Proposed Mixer and Mixers in References

References	**[8]**	**[12]**	**[4]**	**[14]**	**This work**
CMOS Process (µm)	0.6	0.18	0.065	0.13	0.065
Supply Voltage (V)	1.5	1.8	1.8	1	0.8
f_{RF} (GHz)	0.95	1.9	1.9	2.4	2.4
f_{LO} (GHz)	1.275	1.8	1.8	2.3	2.3
Power consumption (mW)	1.4	3.8	2	0.5	5.5
IIP3 (dBm)	-7	-5	6	-9	32
P-1dB (dBm)	NA	-10	-11.5	-28	-18.013
Conversion Gain (dB)	NA	7	12.42	15.7	25.39
Noise Figure	12	8	8.92	18.3	9.236

The overall performance of proposed single balanced RF active mixer can be determined with the help of Figure of Merit (FOM) [14]. The relation between FOM, Gain, noise figure (NF), linearity (IIP3), LO signal power (P_{LO}), operating frequency (f_0) and DC power consumption (P_{DC}) is expressed in Eq.(13).

$$FOM = 10\log\left\{\frac{10^{(Gain-2NF+IIP3-10-P_{LO})/20}\times\frac{f_0}{1GHz}}{\frac{P_{DC}}{1mW}}\right\} \tag{13}$$

Gain represents the conversion of the mixer, f_o represents the 2.4GHz frequency and IIP3 represents the third order intercept point. The figure of merit for the designed mixer is obtained as 6.4dB.

5. CONCLUSION

Thus the single balanced mixer is designed in 65nm CMOS Technology and simulated using ADS tool. The proposed mixer achieves a conversion gain of 25.39dB, minimum noise figure of 8.828dB at IF port and good isolation between ports. It consumes a very low power of 5.5mW. The single balanced mixer designed can be used for many applications like Bluetooth, Zigbee and for many short range wireless communication purposes.

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