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GATE ENGINEERING OF DOUBLE GATE $In_{0.53}Ga_{0.47}As$ TUNNEL FET

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Abstract

Increased power-dissipation in upcoming generation digital systems are limited by supply voltage reductions. For such systems, transistors with lower Subthreshold Slopes are needed. Tunnel Field Effect Transistors (TFET), which works on the principle of band-to-band tunnelling, are supposed to be the possible solution for this problem. TFETs ON-current (I_{ON}) is usually very low, with the use of semiconductors with indirect and large bandgap, and high effective mass as silicon, where tunnelling probability is depressed. One solution to this problem is the use of III-V semiconductors like InAs, GaSb, GaAsSb, $In_xGa_{1-x}As$ etc. and structure of gate is another important factor. Double gate instead of a single gate structure will provide improvement in I_{ON}. Work function of the gate material also has a great impact. In this paper, a study of the impact of $In_{0.53}Ga_{0.47}As$ channel material, gate structure, work function and high-k dielectric for gate for TFET using Cogenda VTCAD is presented.

Keywords:

Band to Band Tunnelling, Double Gate TFET, III-V Semiconductors, High-k Dielectric

1. INTRODUCTION

MOSFET, the metal–oxide–semiconductor field-effect-transistor has been the backbone of an ever increasing number of digital integrated circuits. MOSFET device scaling plays an important role in the rapid development of the semiconductor industry. Device scaling allows for more devices and/or functions to be integrated into a single chip with a given silicon area, or allow the same number of devices or a given function to be realized on a chip with a smaller silicon area. Cost per device and/or per function has been greatly reduced, which is one of the root reasons for the widespread adoption of electronic devices.

Intel cooperation co-founder Gordon Moore, made an observation in 1965 which is now known as the "Moore's Law". It states that the number of transistors being integrated into ICs will increase exponentially, doubling every 2 years. The numbers of MOSFETs integrated into various Central Processing Units (CPUs) followed Moore's Law for the past few decades. More than 100 times reduction in the cost per transistor was achieved in the past 20 years. MOSFETs have also been greatly miniaturized. In order to support the voltage scaling requirement and to reduce the power consumption, new device concepts that can overcome the thermal limit of 60 mV/decade are required.

A transistor with a steeper subthreshold slope (SS) allows for transition from ON to the OFF states over a smaller V_{GS} change, keeping the same I_{ON}/I_{OFF} current ratio. Such devices are potentially useful in both Low Power and High Performance applications. For such systems, we need transistors with SS < 45 mV/decade, or lower, on at least three decades of drain current (I_{DS}). TFET had garnered interests by its steep subthreshold slope, reduced short-channel effects and low power consumption.

In n-TFETs, carrier injection is through the band-to-band tunneling (BTBT) of electrons from a degenerate p+ source into the conduction band of intrinsic channel, so that the semiconductor bandgap filter out the high-energy carriers, hence steeper subthreshold slopes are achieved.

The rest of the paper is organized as follows: Section 2 comprises of the literature review, which covers the major drawbacks of the existing CMOS technology and introduces the TFET. Section 3 deals with $In_{0.53}Ga_{0.47}As$ TFET. Section 4 introduces the double gate TFET architecture, sections 5 and 6 explains briefly, the study of the impact of gate work function and oxide dielectric respectively. And finally section 7 concludes the paper.

2. MOTIVATION AND LITERATURE REVIEW

The first commercial release of a computer based on integrated circuit (IC) technology dates back to late-1960s. The silicon Complementary Metal-Oxide-Semiconductor (CMOS) transistor, currently the most widespread semiconductor switch lies in the heart of this tremendous adventure. The big success of the CMOS devices is explained by the possibility to increase the drive current and the cut-off frequency at the same time only by reducing the size of the devices [1].

2.1 LIMITATIONS OF MOSFET

In spite of its massive use and monopoly in IC industry, MOSFET have quite a few numbers of limitations. The major limitations of MOSFET include subthreshold slope limitations, high leakage current and tunneling currents. Device scaling also leads to shorter gate delay due to an increase in MOSFET drive current with gate length reduction. The dynamic power 'P_{dyn}' and standby power '$P_{standby}$' per device can be described by the following equations:

$$P_{dyn} = f \times C \times V^2_{DD} \quad (1)$$

$$P_{standby} = W \times I_{OFF} \times V_{DD} \quad (2)$$

where, f is the device operation frequency, C is the device load capacitance, W is the device width, I_{OFF} is the off-state leakage current, and V_{DD} is the supply voltage. It is noted that the power consumption for modern ICs needs to be maintained at an acceptable or a sufficiently low level. The fundamental challenge is the steepness of subthreshold slope and next one arising from transistor scaling is the increase of tunneling currents.

2.2 TUNNEL FET

Tunnel FET uses P-I-N structure, the device concept which makes this device different from others is that this device uses quantum-mechanical tunneling phenomenon through the bandgap of semiconductors. In this device the function of the gate electrode is to modulate the potential of i-region so that it can control the

tunneling phenomenon from the source to the channel region [2]. Because of lower subthreshold-swing, tunnel field-effect transistors are potential successors of conventional bulk MOSFETs. Tunnel FET can operate on significantly reduced supply voltage and it seems a promising candidates for low-power operation.

TFET structure is similar to MOSFET, but with opposite type doping in Source and Drain. The simplest TFET is a gated P-I-N diode where the source and drain are highly doped with the gate controlling the band-to-band tunneling between the I-channel region and the P+ or N+ region by way of energy band bending in the I-channel region. In order to be consistent with MOSFET technology, the names of the device terminals are chosen such that voltages are applied in a similar way for Tunnel FET operation [3]. The Fig.2 shows an N-type P-I-N structure TFET. The gate induces an N+ channel to form at the surface of the intrinsic channel region in this case and causes a P+/N+ junction to form at the source to channel interface.

The tunneling probability T_{tunnel} has an expression with Wentzel-Kramers-Brillouin (WKB) approximation as [4].

$$T_{tunnel} = e^{-2\int_0^{w_T} \frac{\sqrt{2m_r^*[U(x)-E_c]}}{\hbar}.dx} \approx e^{-\frac{\sqrt[4]{2m_r^* E_g^{\frac{3}{2}}}}{3q\hbar\xi}} \quad (3)$$

where, w_T is the tunneling width, m_r^* is the reduced tunneling mass, $U(x)$ is the potential energy, $\hbar$ is the reduced Planck constant, E_g is the material band gap, and ξ is the uniform electrical field if triangle potential barrier is assumed. It should be noted that the smaller w_T, E_g and m_r^* are, the higher T_{tunnel} becomes. For a fixed material, E_g and m_r^* are fixed, and w_T is an indicator of T_{tunnel}.

An NTFET is a gated p+ -p- n+ diode, while a PTFET is a gated n+ -n- p+ diode. The gate bias is used to modulate the channel potential of a TFET, and thus to control the BTBT at the interface between the source and the channel as show in Fig.1(a) and 1(b).

The TFET is switched off at low V_{GS} due to the appearance of a bandgap which cuts off the Fermi tail of carrier concentrations. Therefore, I_{OFF} is very low and limited by the junction leakage which includes both the drift current and the Shockley-Read-Hall (SRH) generation. In addition, if the junction at the drain side is abrupt, drain side BTBT could occur at off-state, which also contributes to I_{OFF} of a TFET. At ON-state with high V_{GS} and V_{DS}, the I_{DS} of a TFET is the tunnelling current contributed by the source-side BTBT.

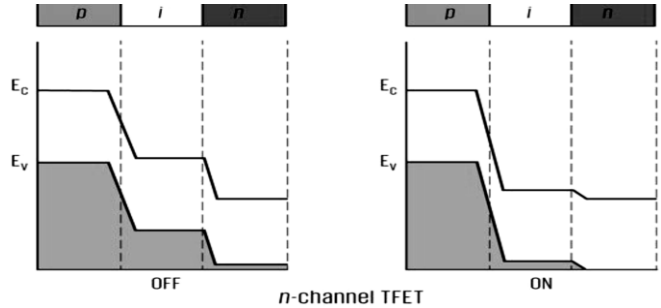

Fig.1. OFF-state (a) and ON-state (b) energy band diagrams of P-i-N TFET [5]

2.3 IMPROVEMENT OF TFET ON CURRENT

In most of the case, the extremely small SS only appears at very low current level although some of the reported TFETs had achieved SS less than 60 mV/decade. Therefore, the existing TFET technology has to improve a lot to become a realistic alternative to CMOS in future. One solution to this problem is the use of III-V semiconductors like InAs, GaSb, GaAsSb, $In_xGa_{1-x}As$ etc.

Another solution to the problem is the gate stack engineering. Gate stack with good interface quality is desirable. Similar to the case in MOSFET, employment of ultra-thin body substrates and multi-gate structures such as nanowire FET [6], could result in better gate modulation of TFETs, enhancing BTBT, improving the tunneling current. Fixing the gate work function to an optimum value is also technique for improvement of I_{ON}. Usage of high-*k* material like HfO_2 in place of SiO_2 will also improve the performance of TFET.

3. InGaAs TFET

Silicon as a channel material bears limits on switching energy, transit time and thermal conductance [7]. Silicon and germanium have indirect bandgap, which means that for the transition from one band to another, electrons must absorb some extra energy from vibrations in the crystal lattice. This significantly lowers the probability that charge carriers will tunnel. As a result, the current carrying capacity of silicon and germanium TFETs are comparatively inferior to III-V compounds. Using channel materials with high mobility increases I_{ON}.

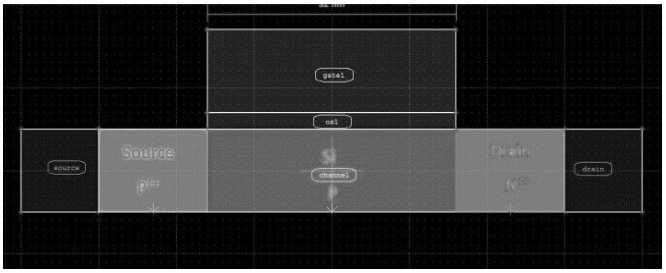

Fig.2. Cogenda simulation structure of single gate Si TFET

According to Hurkx's model [8], which is a modification of the Kanes model [9], the band-to-band generation rate is expressed by,

$$G_{BTBT} = D_{tunnel} \times A_{BTBT} \frac{E^{C_{BTBT}}}{E_g^{1/2}} \times e^{\left(-B_{BTBT} \times \frac{E_g^{3/2}}{E}\right)} \quad (4)$$

where, G_{BTBT} is the band-to-band generation rate, D_{tunnel} is the tunnelling factor that takes into account the probability of having a filled state to tunnel from and an empty state to tunnel to. A_{BTBT}, B_{BTBT} and C_{BTBT} are material related parameters. It can be seen that the material band gap, E_g has an important role in determining the band-to-band generation rate. Materials with a smaller and direct bandgap could greatly increase the band-to-band generation rate and thus increase the TFETs ON current.

The III-V compounds are direct bandgap materials, based on a mix of elements picked from columns III and V of the periodic

table, and are having considerably higher tunnelling probabilities [10]. III-V compound semiconductors like InAs, GaSb, GaAsSb, $In_xGa_{1-x}As$ etc. are commonly used.

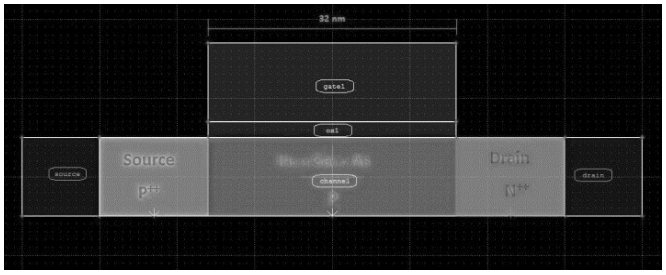

Fig.3. Simulation structure of single gate $In_{0.53}Ga_{0.47}As$ TFET

For our studies we used a III-V turnary compound semiconductor $In_xGa_{1-x}As$ with mole fraction x = 0.47 which is $In_{0.53}Ga_{0.47}As$ as shown in Fig.3. It is having a bandgap of 0.85 eV and effective mass $0.043m_0$, ensuring a higher tunnelling probability. ON current improvement of the $In_{0.53}Ga_{0.47}As$ TFET is shown in Fig.4 which is the plot of V_{GS} against I_D.

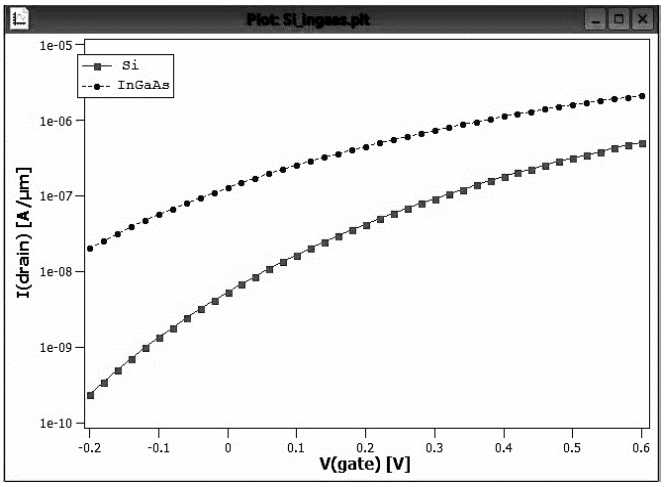

Fig.4. Log I_D-V_{GS} curve for Si and $In_{0.53}Ga_{0.47}As$ TFET

4. DOUBLE GATE $In_{0.53}Ga_{0.47}As$ TFET

As TFETs working principle is gate modulated BTBT, the gate control over the channel surface is an important factor determining the device performance. Study of TFET is more concentrated towards the double gate structure instead of single gate structure. When changing from a single-gate design to a double-gate design, TFETs will benefit from the added control by new gate, such that the current will be at least doubled. In this way, the on-current is significantly boosted, whereas the off-current, increases almost by the same factor but remains extremely low and the device performance does not at all degrades significantly [11]. The main reason behind this is, at low gate bias the tunneling phenomenon takes place at far below the surface and caused low drain current as compared to conventional TFET. However, in high gate bias the tunneling take place at the source-channel junction surface. Hence, for DG TFET the drain current is approximately double because of the presence of both side surfaces compared to its conventional counterpart [12].

Tunneling current is given by,

$$I_{BTBT} \approx \left(-\frac{4\lambda\sqrt{2m^* E_g^{3/2}}}{3\hbar\left(\Delta\phi + E_g\right)} \right) \quad (5)$$

where, m^* is the carrier effective mass, E_g is the semiconductor bandgap, $\hbar$ is the reduced Planck's constant, $\Delta\phi$ is the potential difference and λ is the screening length. λ which is shown in Fig.5, has several different names like natural length and Debye length, and is referred to as the spatial extent of the electric field, or the length over which an electric charge has an influence before being screened out by the opposite charges around it [13].

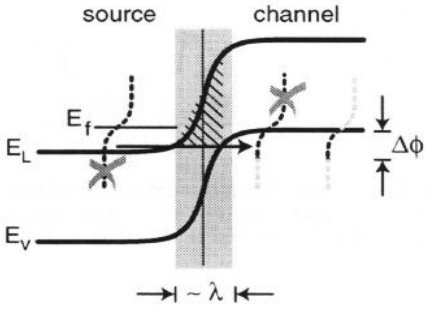

Fig.5. Energy band cross section of Tunnel FET showing λ [14]

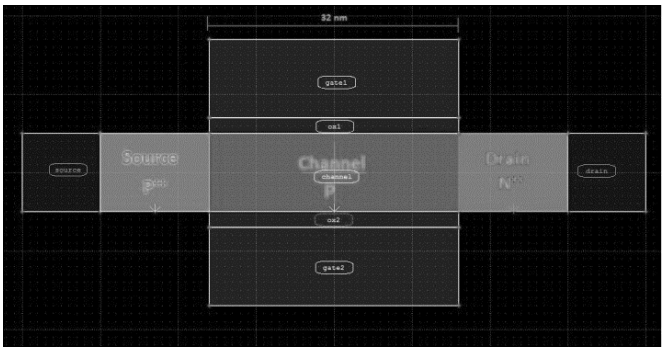

Fig.6. Simulation structure of double gate TFET

In this work, we compare the InGaAs single gate TFET defined in the previous section to a double gate TFET structure with gate length (L_g) = 32 nm and $In_{1-x}Ga_xAs$ with mole fraction x = 0.47 as the channel material as shown in Fig.3. Source, Channel and Drain doping are $1\times10^{20}cm^{-3}$, $1\times10^{16}cm^{-3}$ and $1\times10^{18}cm^{-3}$ respectively. HfO_2 high-k dielectric is used as the gate dielectric with effective oxide thickness (EOT) = 2 nm. Applied V_{DS} is 0.1V, V_{GS} is varied from -0.2V to 0.6V in steps of 0.2V. ON current improvement of the Double gate TFET is evident from the I_D-V_{GS} curves shown in Fig.7.

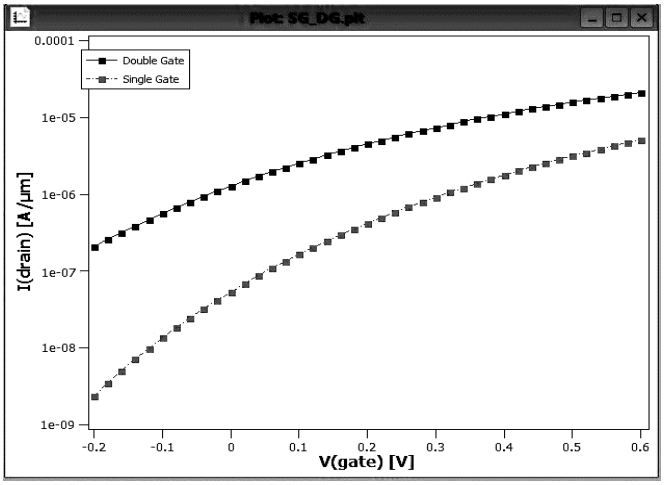

Fig.7. Log I_D-V_{GS} curve for Single and Double Gate TFETs

5. WORK FUNCTION OPTIMIZATION

The work function may be defined as the difference in energy between a lattice with an equal number of ions and electrons, and the lattice with the same number of ions, but with one electron removed. It is assumed in both cases that the lowest electronic states are completely filled, so that the electron is removed from the highest energy state of the neutral metal [15]. Work function has a direct impact on the current characteristics of TFET.

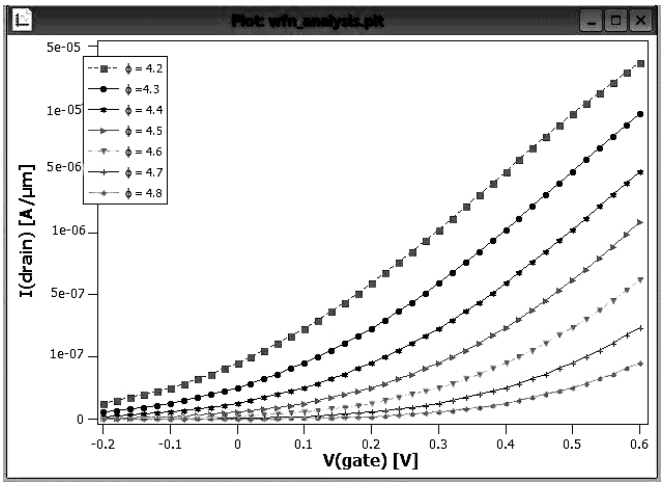

Fig.8. I_D-V_{GS} curve of various work functions for Double Gate TFET

To study the impact of work function we modeled a double gate TFET structure with L_g = 32 nm and $In_{1-x}Ga_xAs$ as channel material with mole fraction x = 0.47 as the channel material as shown in Fig.6. Source, Channel and Drain doping are $1\times10^{20}cm^{-3}$, $1\times10^{16}cm^{-3}$ and $1\times10^{18}cm^{-3}$ respectively. HfO_2 high-k dielectric is used as the gate dielectric with EOT = 2 nm. Applied V_{DS} is 0.1V, V_{GS} is varied from -0.2V to 0.6V in steps of 0.2V. Work function of the gate electrode is varied from 4.2 eV to 4.8 eV and the corresponding I_D-V_{GS} curves are plotted as shown in Fig.8, which clearly indicates the boom in ON current with the reduction in work function.

It is evident from Fig.8 that ON current increases with reduction in work function, but the variation in OFF current is not clear. To have a clear picture of the OFF current logarithm of the drain current is plotted against gate voltage as shown in Fig.9.

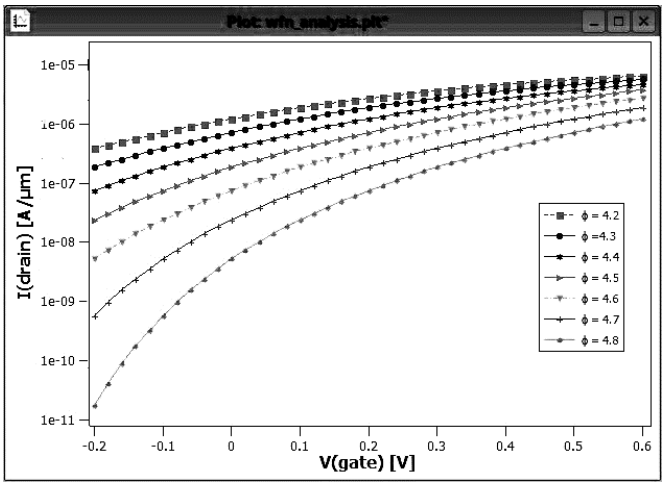

Fig.9. Log I_D-V_{GS} curve of various work functions for Double Gate TFET

It is evident from the figure that, reduction in work function has a hazardous effect on the device OFF current and hence reducing the work function considerably for ON current improvement is not advisable, also higher work functions for reduced OFF current yields poor performance. So we need a tradeoff value for work function, which is in between the extremities.

6. HIGH-K DIELECTRIC

An improved on-current and decreased subthreshold swing can be achieved by the proper choice of agate dielectric. ON current increases as EOT decreases and the gate dielectric constant increases as high-k dielectrics provide better gate coupling [16].

In order to achieve a thin EOT while keeping the gate leakage current low, a high-k material would be needed. For a given EOT, the physical thickness of a gate dielectric layer will be thicker for higher k value as shown below,

$$t_{high-k} = \frac{K_{high-k}}{K_{SiO_2}} \times t_{SiO_2} \tag{6}$$

where, k is the dielectric constant and t is the physical thickness of a dielectric layer. For the analysis a double gate TFET structure with L_g = 32 nm and $In_{1-x}Ga_xAs$ as channel material with mole fraction x =0.47 as the channel material as shown in Fig.3. Source, Channel and Drain doping are $1\times10^{20}cm^{-3}$, $1\times10^{16}cm^{-3}$ and $1\times10^{18}cm^{-3}$ respectively. The EOT of gate dielectric is 2 nm. Applied V_{DS} is 0.1V, V_{GS} is varied from -0.2V to 0.6V in steps of 0.2V.

In this work we have shown the improvement in ON current for the high-k dielectric HfO_2 by plotting the I_D-V_{GS} curve, comparing it with dielectrics such as SiO_2, silicon nitride, and epoxy as shown in Fig.10. The Tunnel FET I_D-V_{GS} characteristics for various gate dielectrics, ε = 2.5 for epoxy, ε = 3.9 for SiO_2, ε = 7.5 for Si_3N_4 and ε = 21 for high-k dielectric HfO_2 are plotted to substantiate the ON current improvement. The curves show that

OFF current of the TFET also increases slightly along with ON current improvement, while including high-*k* dielectric.

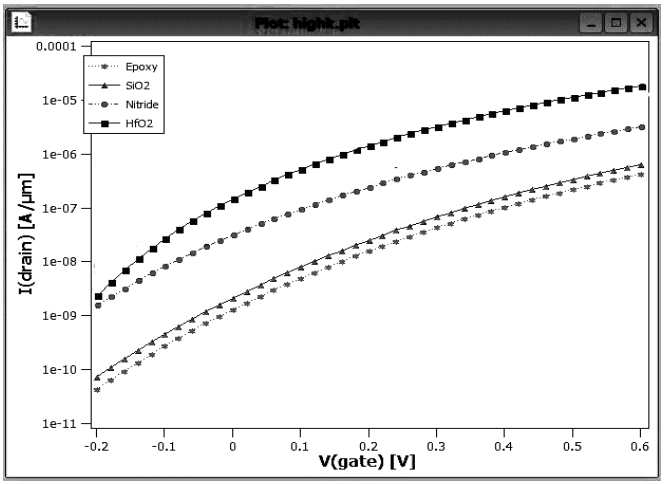

Fig.10. Log I_D-V_{GS} curve for different dielectrics

7. CONCLUSION

TFET is proved to be the number one contender for the throne of CMOS. Even though TFETs have smaller subthreshold slope their I_{ON} is usually very low. One of the possible solutions to improve I_{ON} includes replacement of silicon with materials having lower bandgap and effective mass like $_{.53}Ga_{0.47}As$ and usage of a double gate instead of a single gate structure. Tradeoff in work function of the gate material to an optimum value along with a high-*k* gate dielectric will improve the ON current to a great extend as shown in the results.

TFET is a field of continuing research. Advanced gate engineering includes incorporating hetero dielectrics and dual material gates for further performance improvement. Material engineering includes heterojunction of III–V compounds to improve the ratio of ON current to OFF current. For the most reliable analysis of TFET characteristics, we require very stringent process and variation control for successful fabrication and characterization of such devices.

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