

## Research Article

# A Double-Boost Converter Based on Coupled Inductance and Magnetic Integration

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High-voltage gain converter has a high-frequency use in some industrial fields, for instance, the fuel cell system, the photovoltaic system, electric vehicles, and the high-intensity discharge lamp. In order to solve the problem of the low-voltage gain of traditional boost converter, the double-boost converter with coupled inductance and doubled voltage is proposed, which connects the traditional boost converter in parallel. The voltage gain of the converter is further improved by introducing the voltage-doubled unit of the coupled inductance. Moreover, the clamp capacitor can absorb the leakage inductance in the circuit and reduce the voltage stress of the switch. In addition, two coupled inductors are magnetically collected; then, the loss of the core is analyzed under the same gain. The detailed analysis of the proposed converter and a comparison considering other topologies previously published in the literature are also presented in this article. In order to verify the proposed converter performance, a prototype has been built for a power of 200 W, input and output voltages of 12 and 84 V, respectively, and a switching frequency of 50 kHz. Experimental results validate the effectiveness of the theoretical analysis proving the satisfactory converter performance, whose peak efficiency is 95.5%.

## 1. Introduction

The output voltage of the photovoltaic circuit board is low. A first-level DC converter should be used to connect the grids, which can set the output voltage of the photovoltaic circuit board to reach the voltage requirement of the grid-connected inverter. Meanwhile, due to the influence of light intensity, the output voltage range of the photovoltaic circuit is quite large, so high-gain DC converters have always been one of the research hotspots at home and abroad [1–4].

In addition, in order to achieve a high-voltage gain in a conventional boost converter, a high duty cycle should be used, which may result in high power loss. Most converters are required to operate at a higher duty cycle and a higher number of component counts, making it easier to saturate the topology with inductive cores. This puts limitations on the converter. Literature [5] proposed an optimized integration of active switching inductor configuration, trapezoidal voltage doubling unit combined with regenerative boost configuration, suitable for DC-DC converter with a

wide range of voltage gain in low duty cycle range, because the input clamped peak current can achieve higher voltage gain at a low duty cycle. In literature [6], switching inductance, switching capacitance, and coupled inductance techniques are implemented using three-winding coupled inductance to achieve high-voltage gain with low turns ratio. With the use of a low-voltage stress power switch, through the recovery of leakage energy, the voltage peak on the power switch can be well suppressed so as to improve the efficiency of the system. The proposed converter in literature [7] is composed of a double switching structure, a three-winding coupling inductor, and two voltage multipliers. The double switching structure is beneficial to reduce the voltage stress and current stress of the switch. Clamping capacitors recover energy from leakage inductors, and the problem of inductor leakage and diode reverse recovery is alleviated, improving efficiency. A novel noncoupled high step-up DC-DC converter is presented in literature [8, 9], which combines passive switched capacitance (PSC) network (also known as 2-cell step (SU2C) with ASL network. The ASL-SU2C

converter is formed. The current output feature of ASL-SU2C-CO (which is called in the article ASL-SU2C-CO) and the voltage output (VO) feature of ASL-SU2C-VO are studied, respectively. ASL-SU2C-CO uses fewer switching devices to effectively reduce losses and improve efficiency. There are only two power switches on the current path, and the voltage stress on the active switch is lower. ASL-SU2C-VO has the characteristics of ASL-SU2C-CO and can provide higher static gain, while its switching is subjected to lower voltage stress, which can be better applied in solar and small-scale wind energy systems, storage energy systems, and other applications requiring nonisolated high-order converters. In literature [10], a novel DC/DC converter combining active switch and coupled inductor structure is proposed. The ASL structure reduces the current stress on the switches during the charge interval, the active clamp technology provides zero-voltage transition (ZVT) for all switches, and the leakage inductance can alleviate the reverse recovery problem of the output diode. Literature [11] proposed that the first coupled inductor-based converter employs two-diode capacitor voltage multipliers (VMs) inserted in an innovative way to give it many advantages. The first involves VMs located near the switch and an output circuit, and two VMs work together to provide a very large DC gain. The second method combines forming a new hybrid VM cell with a single VM. The recovery problem of the output diode is eliminated. No spike occurs at its turn-off. Its advantage is eliminating the output diode recovery problem and thus does not result in spikes at its turn-off. In literature [12], a voltage multiplier unit and a switching capacitor unit are combined to achieve low voltage and low current stress efficiency between components. In literature [13–17], a three-phase asymmetric inductor was used to replace a three-phase discrete inductor and an integrated magnetic structure technology was adopted. This reduces the total volume of the core, thus increasing the efficiency of the system. Literature [18] connected the basic boost converter and the voltage-doubled unit in parallel. All stages are activated by the boost switch. Each converter contains a switched capacitor circuit, which has a simple structure and can recover leakage inductance energy. In literature [19], the traditional boost converter and SEPIC converter are used as an alternative structure of the series output module. The boost converter and the SEPIC converter use the same boost inductor and the same switch, which can reduce the input current ripple while maintaining the characteristics of the boost converter. The circuit topology proposed in [20] uses switched capacitor voltage doubler and an integrated LC2D output network to increase the voltage gain of the converter and reduce the voltage stress on the power switch. It has a continuous input current, low-voltage stress on its semiconductor device (less than half of the output voltage), and a constant potential difference between its input and output grounded terminals. The converter is under a wide range of voltage gain and can adapt to the soft output characteristics of the fuel cell. This research proposes a dual boost converter with coupled inductance voltage doubling unit clamped to the ground. In order to effectively improve the voltage gain of the converter, two traditional boost converters are

combined in parallel, the clamp capacitor reduces the voltage stress of the switch tube, and the latter stage of the converter adds a coupled inductance voltage double unit composed of a coupled inductor, a diode, and a capacitor, which improves the gain and reduces the voltage stress of the switch tube. Analysis of the topological structure and working principle of the converter is quite detailed and exhaustive. The theoretical analysis shows that the gain of the converter is related to the turns ratio and the duty cycle of the coupled inductor. The coupled inductor is integrated together. Under the same voltage gain, a different duty cycle is obtained by changing the original and secondary side turns ratio  $n$  of the coupled inductor. The loss of the magnetic core under different duty cycles is analyzed to obtain the highest efficiency of the converter output. A practical 200 W prototype is built to verify the correctness of the theoretical analysis.

## 2. Topological Structure and Working Principle of the Converter

*2.1. Topological Structure.* The topological structure of the converter is shown in Figure 1. Two traditional boost converter topologies are connected in parallel at the input end, and the same structure is combined. The output ends are superimposed in a series to form the front stage of the output converter. The introduction of a coupled inductance voltage-doubled unit in the backstage of the converter further improves the output-input voltage ratio, forming a high-voltage gain boost converter, as shown in Figure 2. On this basis, a clamping capacitor is introduced to absorb the leakage inductance in the coupled inductor and suppress the reverse problem of the diode.

For the convenience of the analysis, the following assumptions are proposed:

- (1) All switching tubes and diodes are ideal devices, both switching tubes and diodes are ideal devices, and the conduction voltage drop is zero
- (2) The coupled inductor is an ideal device, ignoring its parasitic parameters
- (3) The capacitor in the converter is an ideal device, and its capacitance value is large enough to ignore capacitor voltage fluctuations

*2.2. Working Modes of the Converter.* The equivalent circuit of the converter is shown in Figure 3. In a switching cycle, the CCM (continuous conduction mode) of the converter has five working modes, and the working waveforms of each mode are presented in Figure 4. Different working modes of each converter have different equivalent circuit diagrams, as shown in Figure 5:

- (1) Mode I [ $t_0-t_1$ ]: from  $t_0-t_1$ , the switches  $S_1$  and  $S_2$  are closed; the diodes  $D_1$ ,  $D_2$ , and  $D_4$  are off, and  $D_3$  and  $D_5$  are on. The equivalent circuit is shown in Figure 5(a). The excitation current  $i_{Lm}$  starts to rise linearly under the action of the power supply  $V_{in}$ , and the secondary side currents  $i_{L1}$ ,  $i_{L2}$  present a

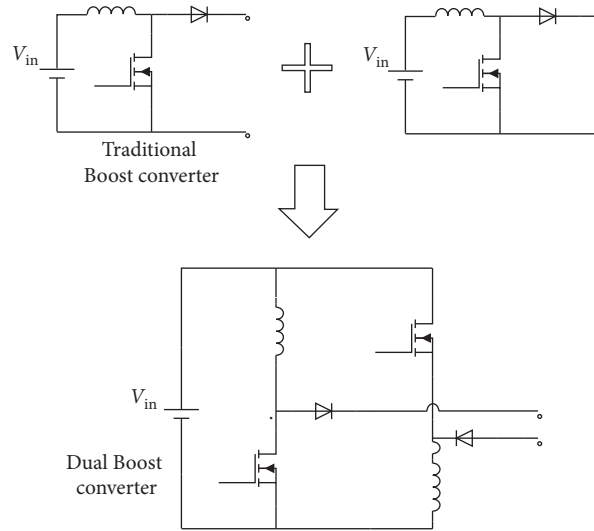


FIGURE 1: Parallel double-boost structure.

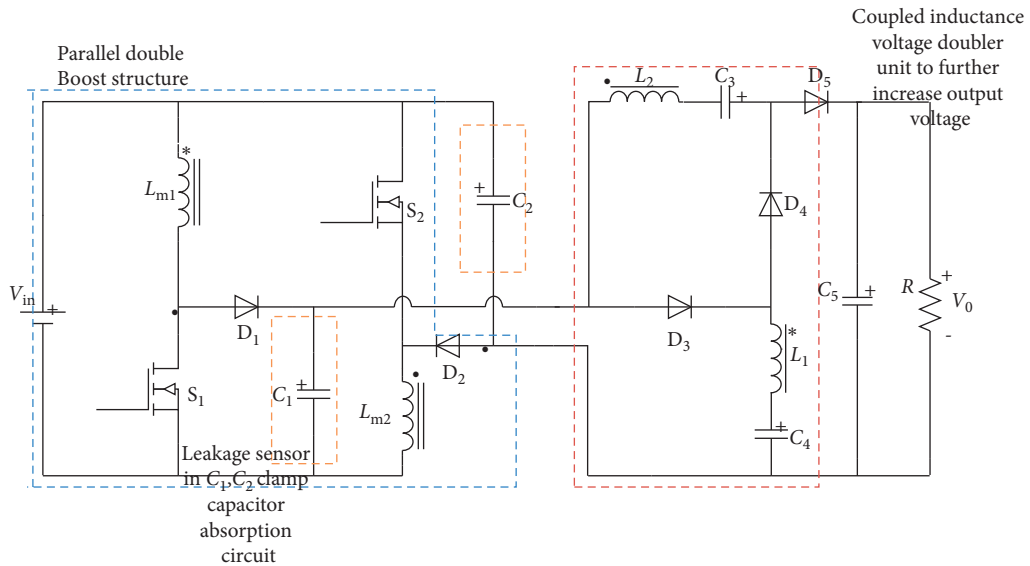


FIGURE 2: Double-boost combined converter with the double-voltage coupled inductor.

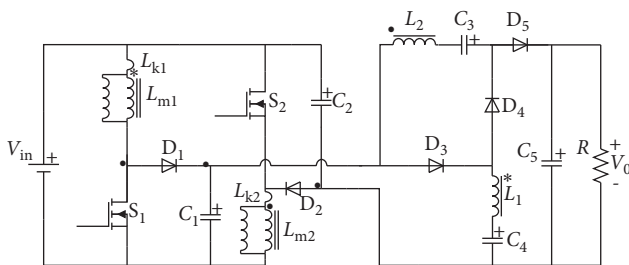


FIGURE 3: Equivalent circuit diagram.

linearly decreased trend. The power supply, along with the primary and secondary sides of the coupled inductor and the capacitors  $C_1, C_2, C_3, C_4$ , provides power to  $C_5$  and the load together. When the secondary side currents  $i_{L1}$  and  $i_{L2}$  drop to 0, the diodes  $D_3$  and  $D_5$  are cut off, and mode I ends.

- (2) Mode II  $[t_1-t_2]$ : from  $t_1-t_2$ , the switches  $S_1$  and  $S_2$  are closed; the diodes  $D_1, D_2, D_3$ , and  $D_5$  are off, and  $D_4$  is on. The equivalent circuit is presented in Figure 5(b). The power supply continues to store energy, and that energy goes to the primary side of the coupled inductor. The leakage current  $i_{Lk}$  and the excitation current  $i_{Lm}$  rise linearly. The power supply, along with the secondary side of the coupled inductor and also the capacitors  $C_1, C_2, C_3, C_4$ , forms a closed loop, and the capacitor  $C_5$  supplies energy to the load alone. Leakage inductance current  $i_{Lk}$  shows a linearly rising trend, and when reaching the maximum state, mode II ends.
- (3) Mode III  $[t_2-t_3]$ : from  $t_2-t_3$ , the switches  $S_1$  and  $S_2$  are off, and the diodes  $D_1, D_2$ , and  $D_4$  are on. The equivalent circuit is presented in Figure 5(c). The leakage inductance current is reversed, which will

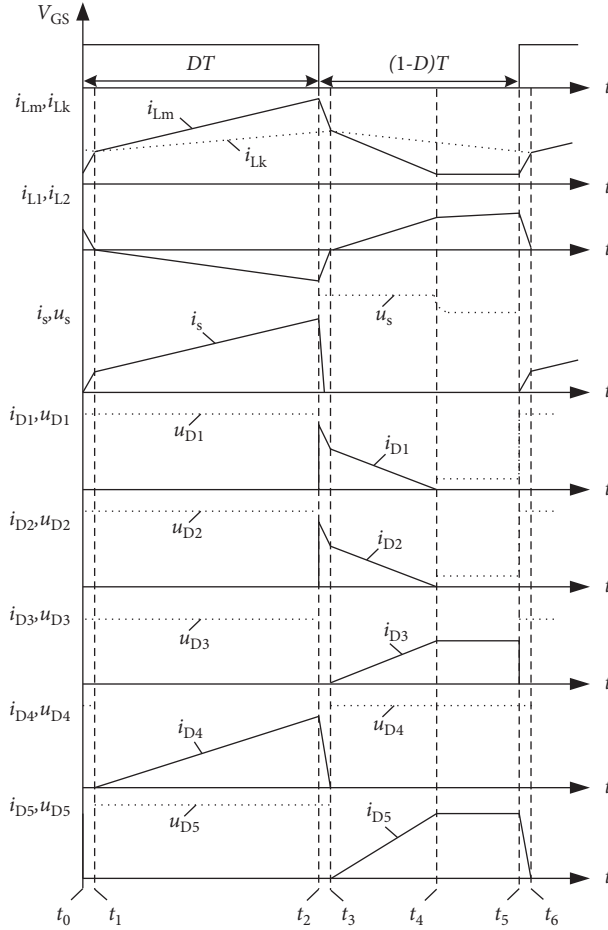


FIGURE 4: Converter operation waveform.

cause a linear decrease of the current on the primary side of the coupled inductor. Capacitors  $C_1$  and  $C_2$  can absorb the leakage inductance in the circuit through diodes, which will result in reducing the voltage stress at both ends of the switch tube; the power supply, the secondary side of the coupled inductor, and also the capacitors  $C_1$ ,  $C_2$ ,  $C_3$ ,  $C_4$  together establish a closed loop. As a result, the secondary side of the current of the coupled inductor will gradually decrease. The capacitor  $C_5$  supplies energy to the load alone. When the secondary side current drops to 0, diode  $D_4$  is off while  $D_5$  is on, and mode III ends.

- (4) Mode IV [ $t_3-t_4$ ]: from  $t_3-t_4$ , the switches  $S_1$  and  $S_2$  are off; the diodes  $D_1$ ,  $D_2$ ,  $D_3$ , and  $D_5$  are on, while  $D_4$  is off. Figure 5(d) shows the equivalent circuit. The leakage inductance current  $L_k$  presents a linearly decreasing trend, as it is consistently absorbed by the capacitors, both  $C_1$  and  $C_2$ . The power supply, the primary and secondary sides of the coupled inductor, the diodes  $D_1$ ,  $D_5$ , and the capacitor  $C_3$  together charge  $C_5$  and power the load; when the current of diodes  $D_1$ ,  $D_2$  drops to 0, the diodes  $D_1$ ,  $D_2$  are off, and modal IV ends.

- (5) Mode V [ $t_4-t_5$ ]: from  $t_4-t_5$ , the switches  $S_1$  and  $S_2$  are off; the diodes  $D_1$ ,  $D_2$ , and  $D_4$  are off, and  $D_3$  and  $D_5$  are on. The equivalent circuit is shown in Figure 5(e). At this time, the capacitors  $C_1$  and  $C_2$  are equivalent to the power supply. The power supply and capacitors  $C_1$ ,  $C_2$ , and  $C_3$  supply energy to the load through the diode  $D_5$ . When the switches  $S_1$  and  $S_2$  are on, mode V ends.

### 3. Performance Analysis

**3.1. Voltage Gain Analysis.** In order to facilitate calculation and analysis, set  $L_{k_1} = L_{k_2} = L_k$ ,  $L_{m_1} = L_{m_2} = L_m$ . The coupling coefficients of the two coupled inductors are both  $k$ , and the coupling coefficient  $k$  can be expressed as follows:

$$k = \frac{L_m}{L_m + L_k}. \quad (1)$$

Assuming that the turns ratios of the coupled inductors are the same, that is,  $n$ , the turns ratio  $n$  can be expressed as follows:

$$n = \frac{n_{s1}}{n_{p1}} = \frac{n_{s2}}{n_{p2}}. \quad (2)$$

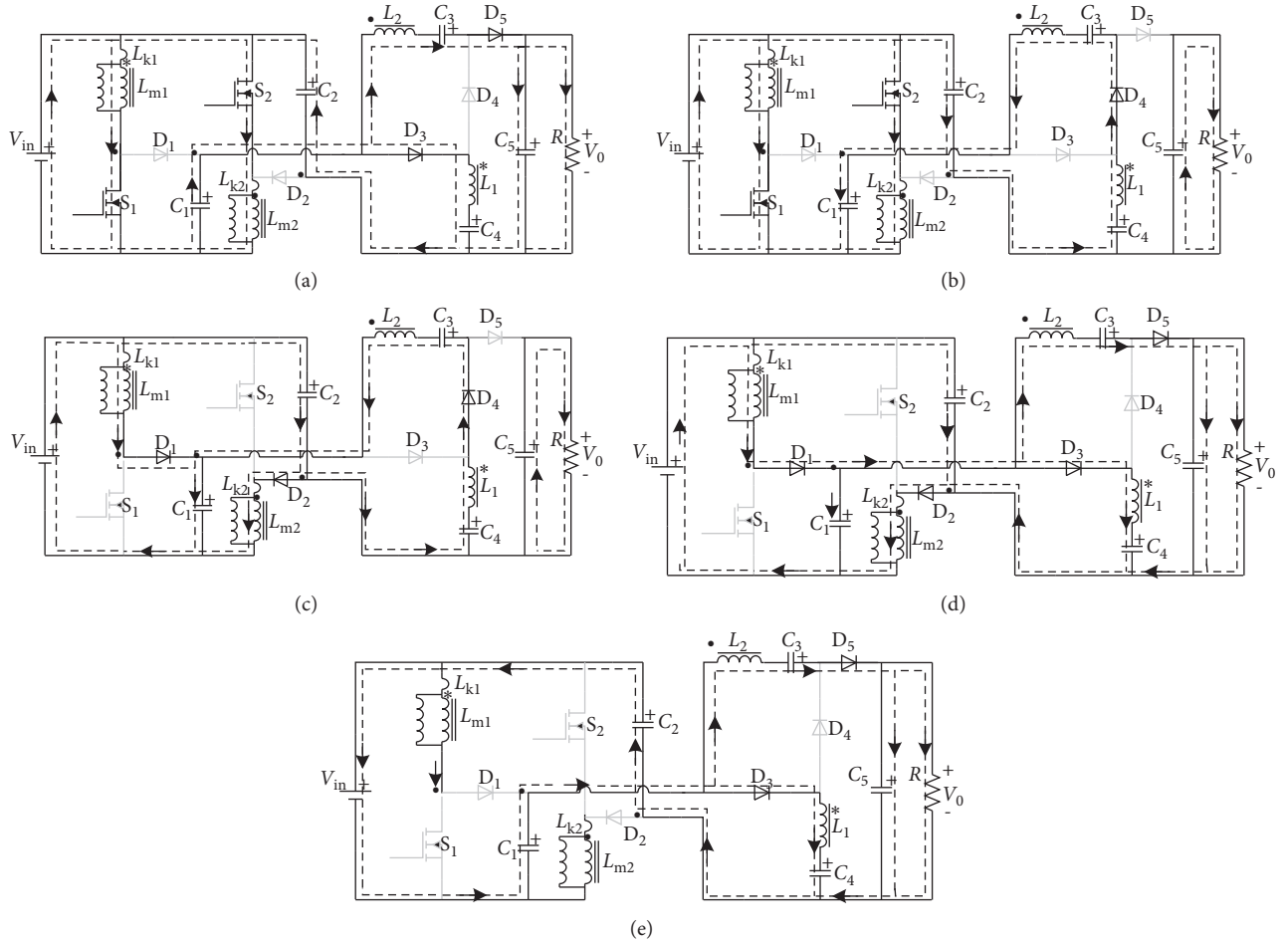


FIGURE 5: Equivalent circuit of each operating mode of the converter. (a) Operating mode I. (b) Operating mode II [ $t_1-t_2$ ]. (c) Operating mode III [ $t_2-t_3$ ]. (d) Operating mode IV [ $t_3-t_4$ ]. (e) Operating mode V [ $t_4-t_5$ ].

The short transition modes I, III, and V are ignored in order to better analyze the steady state. Only modes II and IV are considered here.

In mode II, the loop voltage equation is

$$\begin{cases} V_{L_{m1}} = V_{L_{m2}} = kV_{in}, \\ V_{L_1} = V_{L_2} = nV_{L_{m1}} = nV_{L_{m2}}, \\ V_{C_2} - V_{C_4} - V_{L_1} + V_{C_3} - V_{L_2} + V_{C_1} - V_{in} = 0. \end{cases} \quad (3)$$

In mode IV, the loop voltage equation is

$$\begin{cases} V_{L_{m1}} = k(V_{in} - V_{C_1}), \\ V_{L_{m2}} = k(V_{in} - V_{C_2}), \\ V_{L_{m1}} + V_{L_1} + V_{C_4} + V_{L_{m2}} - V_{in} = 0, \\ V_{L_{m1}} + V_{L_2} - V_{C_3} + V_{C_5} + V_{L_{m2}} - V_{in} = 0. \end{cases} \quad (4)$$

On the grounds of the volt-second balance principle of the coupled inductor  $L_m$ , the following expression of an integral equation is obtained:

$$\int_0^{DT} V_{L_m}^{II} dt + \int_{DT}^T V_{L_m}^{IV} dt = 0. \quad (5)$$

According to equations (1) and (3)–(5), the voltage expression of capacitors  $C_1$  and  $C_2$  is obtained:

$$V_{C_1} = V_{C_2} = \frac{1}{1-D} V_{in}. \quad (6)$$

According to equations (1) and (3), the voltage expression of capacitors  $C_3$  and  $C_4$  is obtained:

$$\begin{cases} V_{C_3} = \frac{2nk - nkD}{1-D} V_{in}, \\ V_{C_4} = \frac{1 + nkD + D}{1-D} V_{in}. \end{cases} \quad (7)$$

According to equations (4), (6), and (7), the voltage gain expression of the converter working in CCM mode is obtained:

$$M = \frac{V_o}{V_{in}} = \frac{1 + D + 2nk}{1 - D}. \quad (8)$$

According to equation (8), there is a strong relationship between the actual gain of the converter, the coupled inductance turns ratio  $n$ , and the coupled coefficient  $k$ . The relationship curve is presented in Figure 6, which shows that

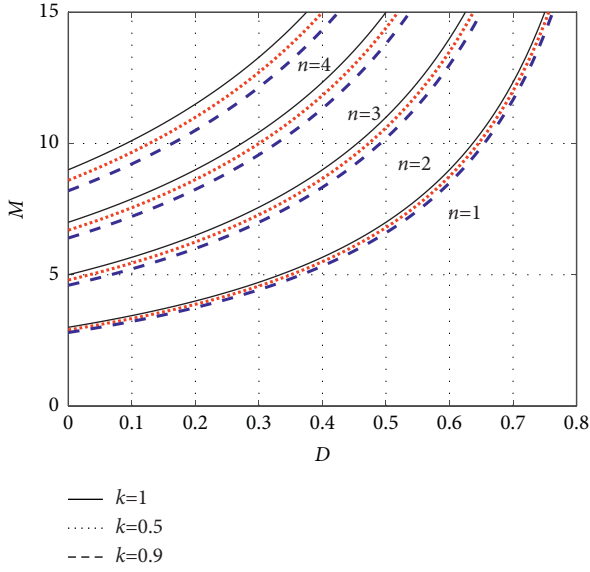


FIGURE 6: Voltage gain of the converter and the coupled coefficient  $k$  and turns ratio  $n$ .

the greater the turns ratio  $n$  of the coupled inductor, the more significant the effect of the converter voltage gain. The increase of the leakage inductance  $L_k$  will result in a reduction to the coupled coefficient  $k$ . In that case, the voltage gain of the converter presents a decreasing trend, which will bring a certain loss of the duty cycle. So in practical applications, the primary and secondary sides of the coupled inductor should be as tightly coupled as possible. Therefore, the higher the coupling degree, the better when the turns ratio is the same.

When  $k=1$ , the voltage gain of the converter is as follows:

$$M = \frac{V_0}{V_{in}} = \frac{1 + D + 2n}{1 - D}. \quad (9)$$

The voltage stress of the switch tubes  $S_1$  and  $S_2$  is

$$V_{vpsS_1} = V_{vpsS_2} = V_{in} - V_{L_m} = \frac{1}{1 + D + 2n} V_o. \quad (10)$$

The voltage stress of diodes  $D_1$  and  $D_2$  is

$$V_{vpsD_1} = V_{vpsD_2} = V_{C_1} = \frac{V_{in}}{1 - D} = \frac{1}{1 + D + 2n} V_o. \quad (11)$$

The voltage stress of diodes  $D_3$  and  $D_4$  is

$$\begin{cases} V_{vpsD_3} = \frac{n}{1 + D + 2n} V_o, \\ V_{vpsD_4} = \frac{2n}{1 + D + 2n} V_o. \end{cases} \quad (12)$$

The voltage stress of diode  $D_5$  is

$$V_{vpsD_5} = \frac{2n - 1 + D + nD}{1 + D + 2n} V_o. \quad (13)$$

According to formulas (10)–(12), the three-dimensional curved surface diagram of the ratio of voltage stress at both

ends of switches  $S_1$ ,  $S_2$  and diodes  $D_1$ ,  $D_2$ ,  $D_3$ ,  $D_4$  to output voltage  $V_{vps}/V_o$ , the coupled inductance turns ratio  $n$ , and duty cycle  $D$  is shown in Figure 7. It can be seen from Figure 7 that the voltage stress of all power devices is less than the output voltage under different duty cycle  $D$  and different turns ratio  $n$ . With the increase of turns ratio  $n$ , the voltage stress of switch tubes  $S_1$  and  $S_2$  decreases gradually, the voltage stress of diodes  $D_1$  and  $D_2$  decreases slowly, and the voltage stress of diodes  $D_3$ ,  $D_4$ , and  $D_5$  increases slowly.

According to the analysis in Section 1 above, the voltage stress of the capacitors  $C_1$ ,  $C_2$ ,  $C_3$ , and  $C_4$  is

$$\begin{cases} V_{C_1} = V_{C_2} = \frac{1}{1 + D + 2n} V_o, \\ V_{C_3} = \frac{2n - nD}{1 + D + 2n} V_o, \\ V_{C_4} = \frac{1 + nD + D}{1 + D + 2n} V_o. \end{cases} \quad (14)$$

The voltage stress of the output capacitor  $C_5$  is

$$V_{C_5} = V_o. \quad (15)$$

The three-dimensional surface diagram of the ratio of voltage stress at both ends of the capacitors  $C_1$ ,  $C_2$ ,  $C_3$ ,  $C_4$  to the output voltage  $V_o$ , the coupled inductance turns ratio  $n$ , and the duty cycle  $D$  is shown in Figure 8. It can be seen from Figure 8 that the voltage stress of all capacitors is less than the output voltage if there are different duty cycle  $D$  and turns ratio  $n$ . The voltage stress of the capacitor  $C_4$  will reduce significantly if the turns ratio  $n$  improves. However, in this case, the voltage stress of the capacitor  $C_3$  will increase greatly. As duty cycle  $D$  increases, the voltage stress of capacitors  $C_1$  and  $C_2$  increases gradually, the voltage stress of  $C_3$  reduces significantly, and the voltage stress of  $C_4$  increases significantly.

**3.2. Comparison of Converter Performance.** This section compares the proposed topology with similar high-gain nonisolated structures, such as the three-winding coupled inductor converter [6], ASL-SU2CCO [8], ASL-SU2CVO [9], ZVT converter [10], and the proposed structure in literature [20–24]. The proposed converter is compared with the revealed topologies in the component counts, voltage gain, and the stress of the power switch, as illustrated in Table 1. Under  $n=2$ , the voltage gain curves versus duty cycle and voltage stress on the power switch versus voltage gain are shown in Figures 9 and 10, respectively. The proposed converter can achieve high-voltage gain with lower voltage stress on the power switch.

## 4. Working Characteristics of Magnetic Components in Converters

**4.1. Preselection of Cores.** It is known that the output power of the coupled converter is 200 W; the efficiency is assumed to be 80%; the working frequency is 50 kHz; the power loss

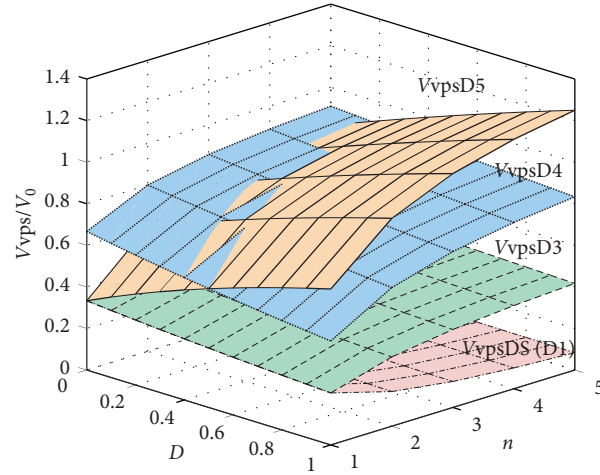
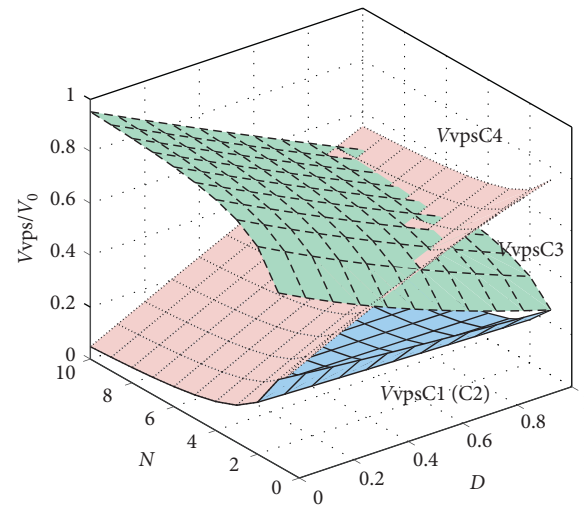
FIGURE 7: The relationship between the voltage stress of switches, diodes, the turns ratio  $n$ , and the duty cycle  $D$ .FIGURE 8: Voltage stress of capacitors, turns ratio  $n$ , and duty cycle  $D$ .

TABLE 1: Performance comparison of different converters.

Topology	Switches count	Diodes count	Capacitors count	Inductors count	Voltage gain ( $M$ )	Power switch voltage stress ( $V_{ds}/V_{in}$ )	Common ground
Proposed	2	4	5	2	$((1 + 2n + D)/(1 - D))$	$(1/(1 + D + 2n))$	No
[6]	2	3	3	1	$((3 + n + D)/(1 - D))$	$((1 + V_o)/4 + n)(1/(1 - D))$	No
[8]	2	2	3	3	$((1 + 3D)/(1 - D))$	$(1/(1 - D))$	No
[9]	2	3	3	2	$((3 + D)/(1 - D))$	$(1/(1 - D))$	No
[10]	4	2	4	1	$((1 + n + D)/(1 - D))$	$(1/(1 + n + D))$	No
[12]	2	5	5	2	$((5 + D)/(1 - D))$	$(1/(1 - D))$	No
[17]	1	4	5	2	$((1 + n + nD)/(1 - D))$	$(1/(1 + n + nD))$	Yes
[18]	1	4	4	1	$((1 + n + nD)/(1 - D))$	$(1/(1 + n + nD))$	Yes
[25]	1	2	3	3	$((3 + D)/(1 - D))$	$(1/(1 - D))$	No
[21]	1	3	4	2	$((2 + n)/(1 - D))$	$((3 + D)/(1 - D))$	Yes
[22]	1	4	4	2	$((1 + n + D)/(1 - D))$	$(1/(2 + n + D))$	Yes
[20]	1	3	5	3	$((1 + 2D)/(1 - D))$	$(1/(1 + 2D))$	No
[23]	1	3	4	2	$((n + 2)/(1 - D))$	$(1/(2 + n))$	Yes
[24]	1	5	7	3	$((2 + 2D)/(1 - D))$	$(1/(2 + 2D))$	No

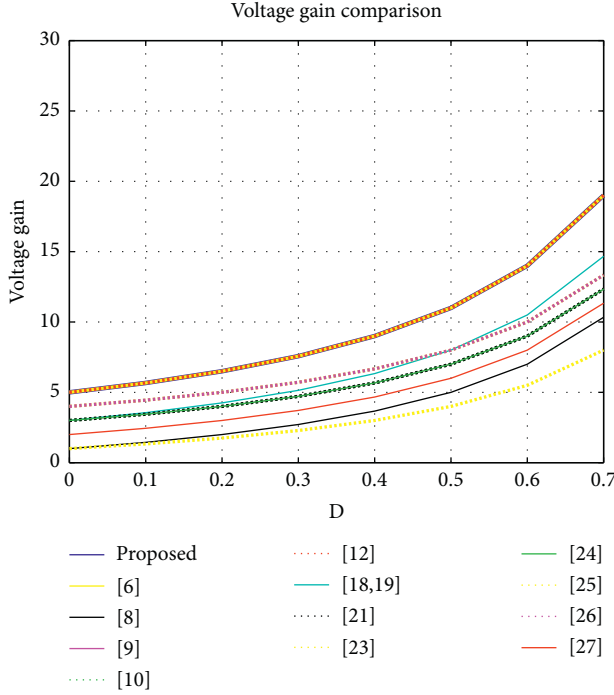


FIGURE 9: Voltage gain comparison curve of the converters.

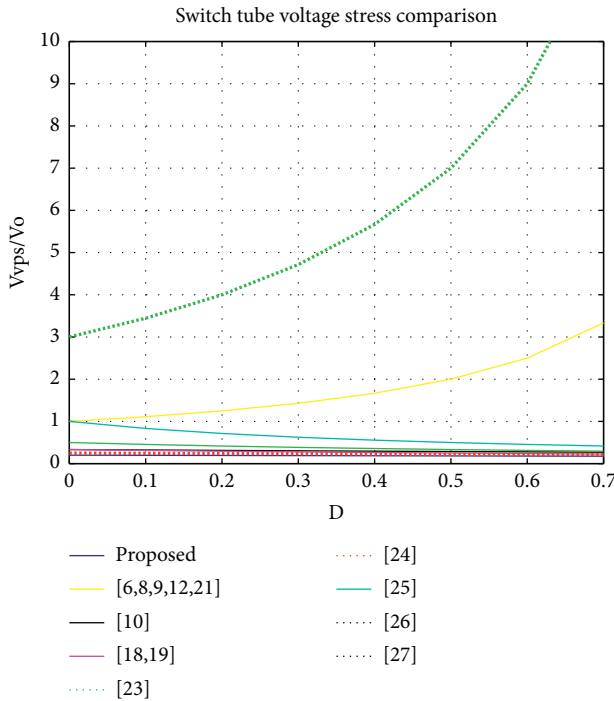


FIGURE 10: Voltage stress comparison curve of converters' switches.

density per unit volume is  $100 \text{ mW/cm}^3$ ; the maximum temperature of the converter is less than  $100^\circ\text{C}$ . Choose the core model suitable for the experiment. The design parameters of the converter are presented in Table 2.

The magnetic core in this article is made of material *F* from the Magnetics company. According to the magnetic core manual, the material has the lowest loss when used at

TABLE 2: Transformer design parameters.

Parameters	Numerical value
Input voltage $V_{in}$ (V)	12
Output voltage $V_O$ (V)	84
Full-load current $i_{FL}$ (A)	9
Magnetic inductance $L$ ( $\mu\text{H}$ )	68
Switching frequency $f$ (kHz)	50
Maximum ripple current $\Delta I$ (A)	11
Peak short circuit current $i_{sp}$ (A)	40
Saturation flux density $B_s$ (T)	0.3

$50^\circ\text{C}$  to  $80^\circ\text{C}$ . According to the AP method, the preselected magnetic core formula is as follows:

$$A_p = A_e \cdot A_w = \left[ \frac{L i_{sp}}{B_s} \cdot \frac{i_{FL}}{K_1} \right]^{(4/3)} \approx 1.45, \quad (16)$$

where  $B_s$  is the saturation magnetic flux density;  $i_{sp}$  is the maximum peak current;  $i_{FL}$  represents the effective value of the full-load current;  $K_1$  stands for the product of the current density and window utilization coefficient, and generally the value is 0.0085. There is a strong connection between the effective cross-sectional area  $A_e$  and the maximum power in the magnetic core.  $A_w$  is the window area where the magnetic core can wind the wire, which is related to the space of the winding. Therefore, within the allowable space, the larger the product of the two, the better. According to the above formula and the actual application, the model PC36 can be selected for experimental verification. The effective parameters of the magnetic core selected in the experiment are shown in Table 3 [26].

**4.2. Design Air Gap Length.** According to the working frequency and output power of the experimental design, the pot-shaped magnetic core is adopted. Considering the convenience of winding manufacturing and the magnetic component installation process, the primary side of the two coupled inductors is tightly wound on the core column, which can better make the secondary side coils closely wound on the surface of the primary side, effectively improving the coupling between the inductors. In order to obtain the required inductance, it is necessary to make the hysteresis loop work in the linear region to avoid saturation of the core and to add an air gap  $\delta$  on the core column. The calculation of the air gap is an approximate iterative process. Assuming that the initial air gap value is  $\delta_0$ , a new air gap value can be obtained by substituting it into the air gap formula  $\delta_1$ . The error between the two air gap values is less than the required value, and the iterative calculation ends.

$$\delta = \mu_0 n^2 \frac{A_e}{L} \left( 1 + \frac{\delta}{D_{cp}} \right)^2. \quad (17)$$

For the selected PC36 magnetic core,  $D_{cp}$  is the diameter of the core column;  $\mu_0$  is the permeability in the air. Assuming the initial air gap length  $\delta_0 = 0.7 \text{ mm}$ , the iterative process is carried out, and the value  $\delta_1$  is obtained by putting the specific data of the magnetic core into formula (17).



TABLE 3: Effective parameters of the magnetic core.

Magnetic parameters	Numerical value
$l_e$ (mm): length of a magnetic path	53.2
$A_e$ (mm <sup>2</sup> ): net sectional area	202
$A_{emin}$ (mm <sup>2</sup> )	172
$V_e$ (mm <sup>3</sup> ): active volume	10700
$A_L$ (nH/T <sup>2</sup> ): inductance coefficient	10200
Outside diameter, inside diameter, height (mm)	35.5, 10.95, 26.2

Compare the values of  $\delta_1$  and  $\delta_0$ , if the error is too large, continue the iteration; when the error is less than 0.4%, stop the iterative process.

$$\delta = 0.75 \text{ mm.} \quad (18)$$

**4.3. Core Loss Simulation Analysis.** In the general calculation of total loss, the loss value is usually ignored, which means that the core loss is roughly regarded as the sum of hysteresis loss and eddy current loss. Figure 11(a) shows the image of the experimental magnetic core, which consists of a cylindrical core of radius  $r$  and length  $l$ . Here,  $dr$  is the differential of the radius  $r$ . Assume that the magnetic flux  $B$  generated by the current is perpendicular to the cross-section upward. The voltage and current waveforms at both ends of the excitation inductance are shown in Figure 11(b).

When sine wave excitation is applied and switches  $S_1$  and  $S_2$  are closed, voltage  $V_{lm}$  and magnetic induction intensity  $B_{sin}$  at both ends of the inductor are follows:

$$\begin{cases} V_{Lm} = V_{in} = L \frac{di}{dt}, \\ B_{sin} = \frac{V_o}{2\pi f n A_e}. \end{cases} \quad (19)$$

When the duty cycle  $D = 0.5$ , under the excitation of the square wave, the relationship between the electromagnetic induction intensity  $B_{0.5}$  and the excitation voltage  $V_o$  can be obtained from the law of electromagnetic induction as follows:

$$B_{0.5} = \frac{V_o T}{4n A_e}. \quad (20)$$

When the duty cycle  $D$  changes, so will the magnetic flux density of the core, and the hysteresis loss generated by the magnetic core will also be different. The magnetic flux density amplitude  $B_0$  is expressed as follows:

$$B_0 = \frac{V_o T [2(n+D)(1-D)]}{n A_e (1+D+2n)^2}. \quad (21)$$

Because the hysteresis loss is proportional to the square of the magnetic flux density [13], under the same working conditions, the hysteresis loss caused by different excitation waveforms is the same.

$$P_h \propto B_0^2 f. \quad (22)$$

According to formulas (21) and (22), the relationship between the hysteresis loss  $P_e$  excited by the rectangular wave and the hysteresis loss  $P_{0.5}$  excited by the duty cycle  $D = 0.5$  is

$$\frac{P_e}{P_{0.5}} = \left( \frac{B_e}{B_{0.5}} \right)^2 = \frac{64(1-D)^2(n+D)^2}{(1+D+2n)^4}. \quad (23)$$

According to formulas (22) and (23), the relationship between the hysteresis loss under rectangular wave excitation and the hysteresis loss under sine wave excitation is

$$\frac{P_e}{P_{sin}} = \frac{64(1-D)^2(n+D)^2}{(1+D+2n)^4}. \quad (24)$$

From Figure 11(a), it can be seen that the expressions of the instantaneous electromotive force, the instantaneous power and the resistance generated by the magnetic core with radius  $R$  are

$$\begin{cases} E = \pi r^2 \frac{dB}{dt}, \\ P_e = \frac{E^2}{R}, \\ R = \rho \frac{2\pi r}{l dr}. \end{cases} \quad (25)$$

According to formula (25), the expression of eddy current loss is

$$P_e = \frac{\pi r^2}{16\pi \rho V_s} \cdot \frac{1}{T} \int_0^T V_{Lm}(t)^2 dt, \quad (26)$$

where  $\rho$  represents the resistivity of the magnetic materials;  $A = \pi r^2$  is the cross-sectional area through which the magnetic flux passes;  $V_s$  is the volume of the magnetic core, which is expressed as  $\pi r^2 l$ . When the circuit is working in a steady state, using the analysis of the working principle of the converters in the first section and the volt-second balance, the following expression can be derived.

$$P_e = \frac{1}{8\pi \rho n^2 A} \cdot \frac{2(1-D)(n+D)}{(1+D+2n)^2}. \quad (27)$$

When the duty cycle of the boost converter and the value of the duty cycle change, the square wave excitation is 0.5 and the expression of the eddy current loss is

$$\frac{P_e}{P_{0.5}} = \frac{8(1-D)(n+D)}{(1+D+2n)^2}. \quad (28)$$

Under the same working conditions, the relationship between the rectangular wave excitation eddy current loss  $P_e$  and the sinusoidal excitation eddy current loss  $P_{sin}$  is

$$\frac{P_e}{P_{sin}} = \frac{16(1-D)(n+D)}{\pi^2(1+D+2n)^2}. \quad (29)$$

When the magnetic core of the converter works in the pulse-width modulation (PWM) waveform, the bias current

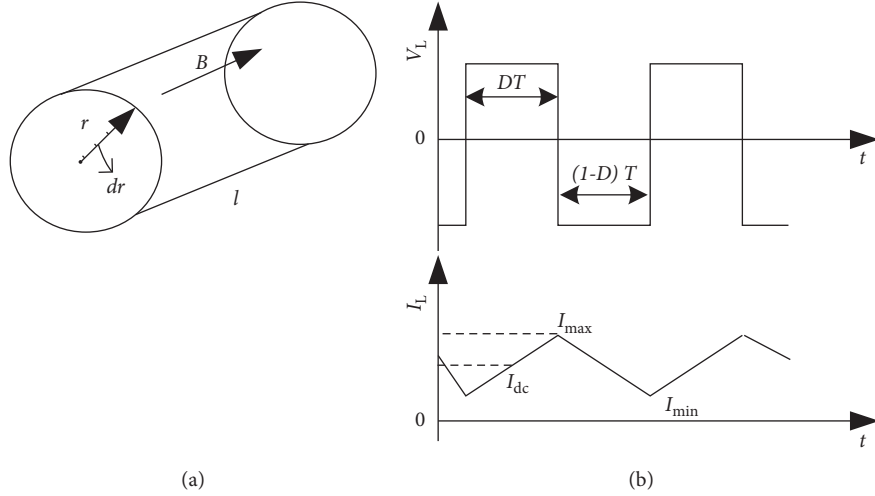


FIGURE 11: Core analogy diagram and excitation inductance voltage and current diagram.

$I_{dc}$  will be generated, and the corresponding hysteresis loss will increase significantly. When different excitation waveforms produce the same magnetic flux density under the same conditions, even under the DC bias condition, the hysteresis loss will have a similar value. Therefore, the DC bias factor  $k_{dc}$  is proposed to show the effect of DC bias on the hysteresis loss, and  $k_{dc}$  is only related to magnetic materials.

$$k_{dc} = \frac{P_e}{P_{sin}}. \quad (30)$$

According to formulas (24), (29), and (30), the core loss of boost converter under different duty cycle conditions can be expressed as follows:

$$P_e = k_{dc} \frac{64(1-D)^2(n+D)^2}{(1+D+2n)^4} P_{sin} + \frac{16(1-D)(n+D)}{\pi^2(1+D+2n)^2} P_{sin}. \quad (31)$$

Ansoft Maxwell is used here for the finite element simulation. Assuming that the parameters of the two coupled inductors are the same and the voltage gain  $M$  is the same, the corresponding duty cycle  $D$  can be obtained by adjusting the winding turns ratio  $n$  of the primary and secondary sides, and the core loss is analyzed under different duty cycles.

**4.4. Simulation of Core Loss.** The magnetic core parameters are analyzed with a frequency  $f$  of 50 kHz, the coupled inductance turns ratio  $n$  of 1, and the duty cycle  $D$  of 0.5. The magnetic flux density of the magnetic core  $B_m$  is 0.30884 T and the core loss simulation results are shown in Figure 12.

Secondly, the model is verified and analyzed when the duty cycle is not 0.5. Frequency  $f$  is still unchanged, and the value of the turns ratio  $n$  in the primary and secondary sides is 2; thus, the core loss with the magnetic flux density  $B_m = 2.519 \times 10^{-2}$  T is shown in Figure 13. The value of the turns ratio  $n$  in the primary and secondary sides is 1.5, the core loss

with the magnetic flux density  $B_m = 2.5198 \times 10^{-2}$  T is shown in Figure 14. Table 4 is the analysis and comparison of the theoretical calculation results and the simulation results. It can be seen that the model proposed in this article can accurately evaluate the core loss under different duty cycles.

**4.5. Loss Analysis.** The analytical loss analysis of the proposed converter is performed by considering the parasitic elements of the components. MOSFETs' losses comprise conduction losses ( $P_{cond}$ ) and switching losses ( $P_{sw}$ ), calculated as follows:

$$\begin{aligned} P_{cond,S_1} &= R_{DS(on)} I_{S_1(rms)}^2, \\ P_{cond,S_2} &= R_{DS(on)} I_{S_2(rms)}^2, \\ P_{sw,S_1} &= f_{sw} V_{S_1} \left( C_{oss} V_{S_1} + \frac{1}{2} I_{Lm1} (t_{on} + t_{off}) \right), \\ P_{sw,S_2} &= f_{sw} V_{S_2} \left( C_{oss} V_{S_2} + \frac{1}{2} I_{Lm2} (t_{on} + t_{off}) \right), \\ P_S &= P_{cond,S_1} + P_{cond,S_2} + P_{sw,S_1} + P_{sw,S_2}. \end{aligned} \quad (32)$$

The conduction losses of the diodes are calculated by

$$\begin{aligned} P_{cond,D_1} &= V_{F0,D_1} I_{D_1(Avg)} + R_{on,D_1} I_{D_1(rms)}^2, \\ P_{cond,D_2} &= V_{F0,D_2} I_{D_2(Avg)} + R_{on,D_2} I_{D_2(rms)}^2, \\ P_{cond,D_3} &= V_{F0,D_3} I_{D_3(Avg)} + R_{on,D_3} I_{D_3(rms)}^2, \\ P_{cond,D_4} &= V_{F0,D_4} I_{D_4(Avg)} + R_{on,D_4} I_{D_4(rms)}^2, \\ P_{cond,D_5} &= V_{F0,D_5} I_{D_5(Avg)} + R_{on,D_5} I_{D_5(rms)}^2, \\ P_D &= P_{cond,D_1} + P_{cond,D_2} + P_{cond,D_3} \\ &\quad + P_{cond,D_4} + P_{cond,D_5}. \end{aligned} \quad (33)$$

The conduction losses of the capacitors are calculated by

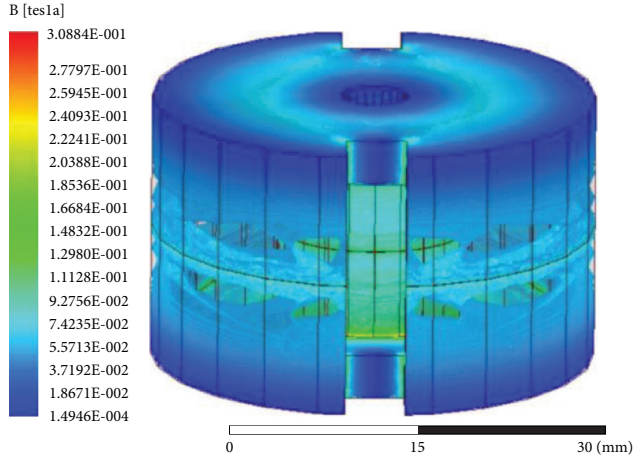
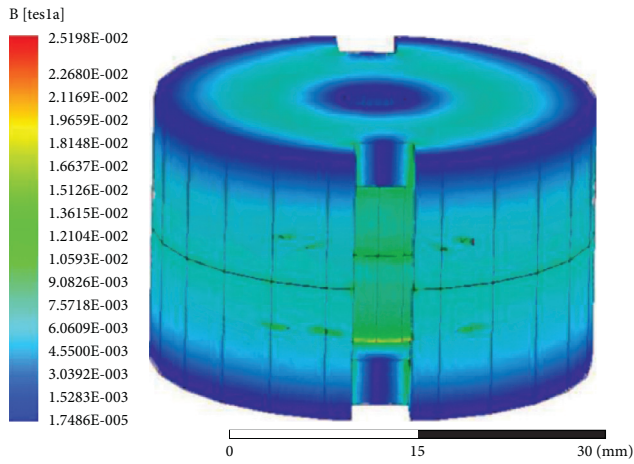
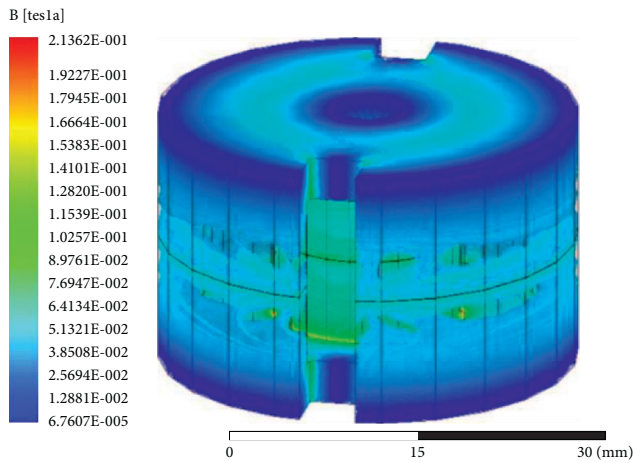
FIGURE 12: Core simulation with duty cycle  $D=0.5$ .FIGURE 13: Core simulation with duty cycle  $D=0.25$ .FIGURE 14: Core simulation with duty cycle  $D=0.375$ .

TABLE 4: Core loss comparison.

Duty cycle $D$	Core loss $W$	
	Simulation result	Calculation result
0.25	$2.417 \times 10^{-4}$	$2.932 \times 10^{-4}$
0.375	$4.955 \times 10^{-2}$	$6.178 \times 10^{-2}$
0.5	$1.393 \times 10^{-1}$	$1.824 \times 10^{-1}$

$$\begin{aligned}
 P_{C_1} &= R_{C_1} I_{C_1(\text{rms})}^2, \\
 P_{C_2} &= R_{C_2} I_{C_2(\text{rms})}^2, \\
 P_{C_3} &= R_{C_3} I_{C_3(\text{rms})}^2, \\
 P_{C_4} &= R_{C_4} I_{C_4(\text{rms})}^2, \\
 P_{C_5} &= R_{C_5} I_{C_5(\text{rms})}^2, \\
 P_C &= P_{C_1} + P_{C_2} + P_{C_3} + P_{C_4} + P_{C_5}.
 \end{aligned} \tag{34}$$

Coupled inductors losses include copper losses ( $P_{\text{cu}}$ , CI) and core losses ( $P_e$ , CI):

$$\begin{aligned}
 P_{\text{cu,CI}_1} &= R_{P_1} I_{L_{k1}(\text{rms})}^2, \\
 P_{\text{cu,CI}_2} &= R_{P_2} I_{L_{k2}(\text{rms})}^2, \\
 P_{\text{CI}} &= P_{\text{cu,CI}_1} + P_{\text{cu,CI}_2} + P_{e,\text{CI}_1} + P_{e,\text{CI}_2}, \\
 P_{\text{Loss}} &= P_S + P_D + P_C + P_{\text{CI}}.
 \end{aligned} \tag{35}$$

The analytical efficiency of the converter is obtained from

$$\eta(\%) = 100 \times \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{Loss}}}. \tag{36}$$

When  $f_{\text{sw}} = 50$  kHz and existing data are substituted into the formula, the final total loss can be obtained as  $P_{\text{Loss}} = 7.46$  W, including  $P_S = 2.96$  W,  $P_D = 3.34$  W,  $P_{\text{CI}} = 0.36$  W, and  $P_C = 0.8$  W (the loss of coupling inductance is calculated at duty cycle  $D = 0.5$ ).

## 5. Experimental Results and Analysis

**5.1. Circuit Experimental Verification.** To verify the correctness of the principles in this article, a 200 W experimental prototype was made in the laboratory. The parameters of the experimental prototype are as follows: input voltage  $V_{\text{in}} = 12$  V, switching frequency  $f = 50$  kHz, capacitance  $C_1 = C_2 = C_3 = C_4 = 100 \mu\text{F}/50$  V,  $C_5 = 100 \mu\text{F}/250$  V, load  $R = 100 \Omega$ . Coupled inductance turns ratio  $n$  is 1. The coupled inductor adopts the tank-type soft ferrite PC36 core. The main circuit parameters are shown in Table 5.

Figure 15 shows the input and output waveforms of the converter. It can be seen that the converter achieves a high-gain conversion of 12 V input and 84 V output, which conforms to the theoretical analysis. Figure 16 shows the driving waveforms

TABLE 5: Main circuit parameters.

Experimental parameters/components	Number/model
Input voltage $V_{in}$ (V)	12
Output voltage $V_o$ (V)	84
Rated power $P_o$ (W)	200
Coupled inductance turn $n$	$n_s/n_p = 1:1$
Inductance $L_1$ ( $\mu\text{H}$ )	68
Inductance $L_2$ ( $\mu\text{H}$ )	67.8
Leakage inductance $L_k$ ( $\mu\text{H}$ )	1.28
Capacitance $C_1/C_2/C_3/C_4$	100 $\mu\text{F}/50\text{ V}$
Output capacitance $C_5$	100 $\mu\text{F}/250\text{ V}$
Switch tube $S_1/S_2$	IRF540N
Diode $D_1/D_2$	MBR20100CT
Diode $D_3/D_4$	MBR20100CT
Diode $D_5$	MBR20100CT
Switching frequency $f$ (kHz)	50

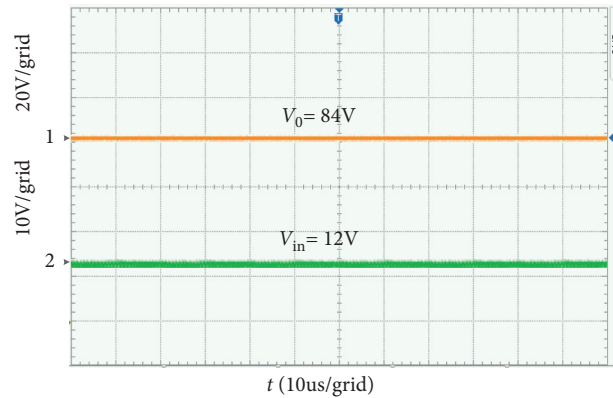
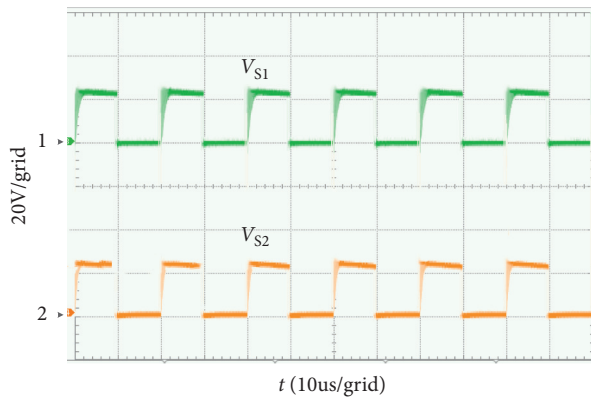
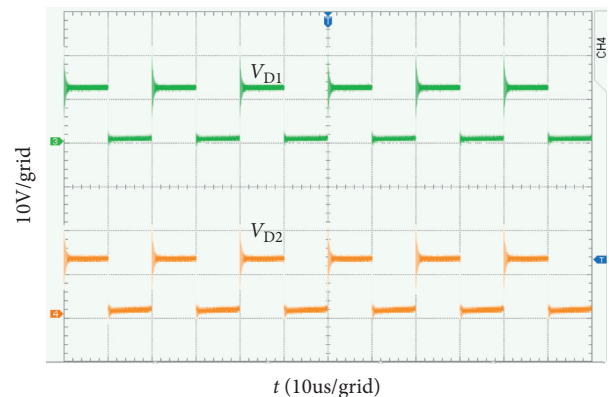


FIGURE 15: Output/input waveform.

FIGURE 16: Waveform of  $V_{s1}$  and  $V_{s2}$ .FIGURE 17: Waveform of  $V_{D1}$  and  $V_{D2}$ .

of the two switch tubes of the converter. Figures 17 and 18, respectively, indicate the voltage stress waveform diagrams of the diode. It can be seen from the figure that the voltage stress of the switch and the diode are less than the output voltage, and the converter has relatively small voltage stress.

Figure 19 shows the current waveforms of the coupled inductor and the switching tube. Figures 20 and 21 show the current waveforms of the main diodes. It can be seen that the diodes have achieved zero current cutoff, and the

theoretical analysis is confirmed by all the experimental results.

When the output voltage is constant at 84 V, the efficiency curve of the converter is obtained by changing the power load, as shown in Figure 22. The load can be adjusted and tends to be stable when the efficiency of the prototype keeps increasing. When the output power increases, so does the efficiency of the prototype. Moreover, when the output power is equal to 50 W, the efficiency of the prototype is the highest, about 95.5%.

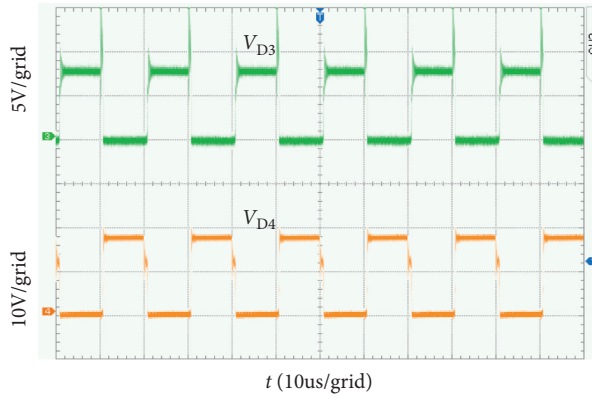


FIGURE 18: Waveform of  $V_{D3}$  and  $V_{D4}$ .

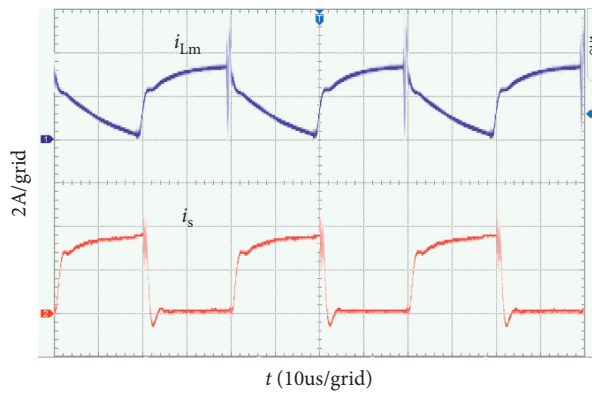


FIGURE 19: Coupled inductor/switch waveform.

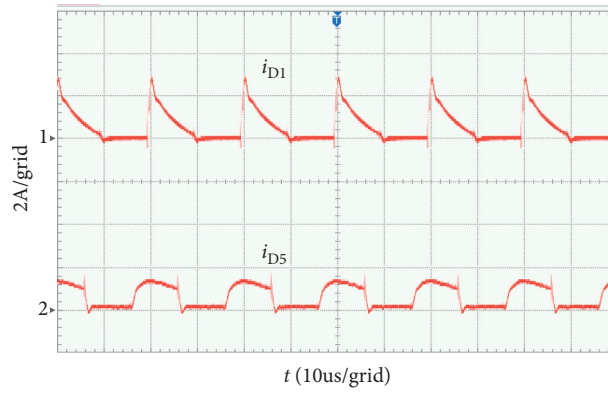


FIGURE 20: Waveform of  $i_{D1}$  and  $i_{D5}$ .

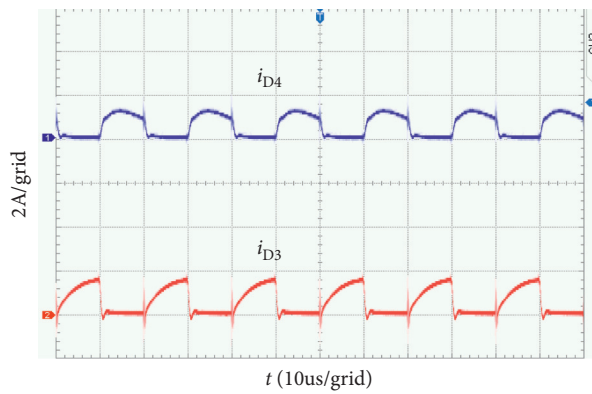


FIGURE 21: Waveform of  $i_{D3}$  and  $i_{D4}$ .

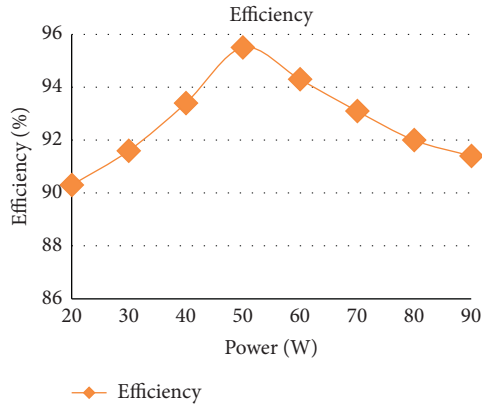


FIGURE 22: Efficiency curve of the prototype.

## 6. Conclusion

On the basis of the parallel double-boost structure, a unit with coupled inductance and doubled voltage is proposed, as well as a new type of converters with high-gain and low-voltage stress. Moreover, the voltage gain of the coupled inductance high-gain converter in CCM mode, along with the voltage stress of switches and diodes, is derived. Secondly, a core loss model of the converter is formed and then verified through the finite element simulation results. Experimental analyses and verification are done and the converter proposed in this article has the following features:

- (1) A coupled inductance doubled-voltage unit is introduced into the converter, which greatly improves the voltage gain and simplifies the design difficulty of the converter.
- (2) The leakage inductance in the coupled inductor affects the parasitic capacitance generated by the converter. The clamping capacitor can absorb the energy of the leakage inductance in the coupled inductor, which can effectively reduce the voltage impulse in the switch tube.
- (3) Taking ferrite magnetic materials as the research object, while maintaining the same voltage gain, the core loss modeling calculation of the converter is compared with the finite element analysis; the core loss of the converter is evaluated; the model of core loss analysis and modeling is correct.
- (4) If the converter is used in a special case (PV systems), techniques for reducing common-mode voltage and leakage current must be employed since, in the proposed converter, there is no common ground between the input and output.

## Data Availability

The theory of data used to support the findings of this study is included within the article.

## Conflicts of Interest

The authors declare that they have no conflicts of interest.

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